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DC offset rejection in a frequency-fixed second-order generalized integrator-based phase-locked loop for single-phase grid-connected applications

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Abstract

Fast and accurate monitoring of the phase, amplitude, and frequency of the grid voltage is essential for single-phase grid-connected converters. The presence of DC offset in the grid voltage is detrimental to not only grid synchronization but also the closed-loop stability of the grid-connected converters. In this paper, a new synchronization method to mitigate the effect of DC offset is presented using arbitrarily delayed signal cancellation (ADSC) in a second-order generalized integrator (SOGI) phase-locked loop (PLL). A frequency-fixed SOGI-based PLL (FFSOGI-PLL) is adopted to ensure better stability and to reduce the complexity compared with other SOGI-based PLLs. A small-signal model of the proposed PLL is derived for the systematic design of proportional-integral (PI) controller gains. The effects of frequency variation and ADSC on the proposed PLL are considered, and correction methods are adopted to accurately estimate grid information. The simulation results are presented, along with comparisons to other single-phase PLLs in terms of settling time, peak frequency, and phase error to validate the proposed PLL. The dynamic performance of the proposed PLL is also experimentally validated. Overall, the proposed PLL has the fastest transient response and better dynamic performance than the other PLLs for almost all performance indices, offering an improved solution for precise grid synchronization in single-phase applications.

Keywords: Grid integration, Virtual microgrid, DC offset mitigation, Grid synchronization, Phase-locked loop, Second-order generalized integrator

1 Introduction

Renewable energy sources are integrated into the grid using grid-synchronized voltage source converters. A precise grid synchronization algorithm influences the power, quality, and reliability of the grid. However, many issues must be overcome to avoid synchronization-related problems. The presence of DC offset in the grid voltage is considered a significant problem, affecting the operation of grid-connected converters and power quality [1–3].

Voltage and current sensors, signal conditioning circuits, quantification errors in the analog-to-digital-conversion process, the mismatch of power semiconductor parameters, and current circulating between inverters are considered the major causes of DC offset in grid voltage [2–10]. The presence of DC offset not only deteriorates the performance of grid synchronization units but also affects the closed-loop stability of grid-connected converters because of oscillations in the estimated grid frequency, phase, and voltage amplitude [2–4].

Much published research is related to orthogonal signal generation (OSG) methods used with single-phase phase-locked loops (PLLs) to create fictitious quadrature signals. Among the many reported OSG-based PLLs,

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the second-order generalized integrator (SOGI) PLL has become the most popular for single-phase applications because of its low computation burden, straightforward implementation, and high filtering capability for low-order harmonics [1–4, 11, 12].

The SOGI-PLL uses an OSG block to generate orthogonal signals from the single-phase grid voltage [2]; to implement the synchronization function, these are fed to the synchronous reference frame-based PLL (SRF-PLL) [13]. To ensure the accurate detection of frequency, voltage amplitude, and phase angle, the estimated SRF-PLL frequency is fed back to the SOGI block, making the SOGI-PLL frequency adaptive. However, this feedback increases the complexity of the design, and the design of loop filter gains becomes difficult [14].

Several SOGI-based PLLs have been reviewed in terms of their ability to remove the effect of DC offset from the grid synchronization process [4, 7]. These methods include the cascaded SOGI-PLL, modified SOGI-PLL, $\alpha\beta$ DSC₂ with SOGI-PLL, in-loop dq-frame DSC, complex-coefficient filter, notch filter, and moving average filter-based SOGI-PLL. The $\alpha\beta$ DSC₂, SOGI-PLL, and modified SOGI-PLL have the shortest settling time when removing DC offset compared with the other SOGI-PLLs. However, all these PLLs have a slow dynamic response, and the closed-loop transfer function is of the third-order, which complicates controller design.

Reference [6] proposes a cascaded generalized integrator (CGI)-based PLL consisting of two cascaded SOGI blocks. To reject DC offset, an SRF-PLL adopting a frequency-fixed procedure is used to ensure stability and simple implementation. The two parameters that must be carefully adjusted to avoid affecting the PLL's transient performance and harmonic filtering capability are designed to minimize the overall settling time of the PLL. However, because CGI-PLL suffers from attenuation to low-order harmonics, the SRF-PLL bandwidth must also be carefully selected to avoid unbalancing the quadrature signals. Also, using two SOGI blocks in a cascade to remove DC offset increases the system's complexity. In [15], a dual SOGI and moving average filter in-loop with the SRF-PLL are combined to form a hybrid filter-based PLL. This method blocks the fundamental frequency negative sequence component, DC offset, and dominant harmonic components and has a relatively fast transient response. However, the transient response performance depends on the window length of the hybrid filter.

A mixed second-and third-order generalized integrator (MSTOGI)-based PLL is presented in [16, 17]; it contains an extra branch to the SOGI block to eliminate DC offset and high-frequency harmonics from input signals. The MSTOGI gain affects the filtering capability, dynamic performance, and bandwidth of the SRF-PLL.

Therefore, the MSTOGI-PLL controller gain has to match the MSTOGI gain to maintain stability and optimize the settling time. The dynamic performance of the MSTOGI-PLL is proportional to its bandwidth, so a high bandwidth must be chosen to achieve a faster transient response. However, a higher bandwidth weakens the ability to suppress low-frequency harmonics in the grid voltage. The system stability and pole trajectory aspects of generalized SOGI and TOGI-based PLLs have been investigated in [18]. Although a TOGI has advantages over a SOGI under harmonically distorted grid conditions, it is more complicated than a SOGI.

In [19], a frequency-locked loop (FLL) control method is used to eliminate DC offset, in which the FLL controller is combined with a modified SOGI block to estimate and obliterate DC offset from grid voltage. In general, since frequency adaptation is highly nonlinear, the linear control analysis technique cannot be directly applied, and thus it increases the design complexity. Also, the dynamic response of the SOGI-FLL depends on the adequate selection of the FLL and SOGI gains. The complexity and computational burden of frequency-fixed SOGI-based PLL (FFSOGI-PLL) is notably reduced compared with the classical SOGI-PLL. This allows for higher bandwidth, better stability margin, and faster dynamic response. However, with grid frequency variation, FFSOGI-PLL suffers from double-frequency harmonics related to bandwidth selection [20].

The SOGI-FLL with fixed frequency proposed in [21] incorporates a low pass filter with notch characteristics and a linearized phase error compensation to mitigate the double-frequency oscillation in the estimated grid information. Although this FLL has straightforward parameter tuning and selective harmonic rejection capability based on a linearized phase-loop transfer function, it has limited DC offset rejection capability. In [22], a solution is proposed for the double-frequency term and offset error in the frequency-fixed SOGI using a conformal mapping-based fractional-order approach. The PLL shows good dynamic performance during different disturbances, including DC offset, by adjusting the fractional-order gain according to grid frequency variations. However, the use of fractional-order calculus increases system complexity and computational burden. A discrete-time non-adaptive SOGI-FLL based on a gradient descent algorithm is presented in [23]. Although its dynamic performance is smooth and fast, the method cannot completely reject DC offset.

A type 3 modified SOGI-PLL is presented in [24], addressing the slow dynamic response, instability under voltage sag, and poor damping under other abnormal grid conditions by enhancing the gain and phase margins using gain and phase-lead compensators. This PLL

converges within two grid cycles under frequency, phase, and voltage sag disturbance. However, it cannot reject the DC offset. A modified version has been presented in [25] to add a DC offset rejection capability to the PLL using the notch filter. A trade-off between the filtering capability and dynamic performance is recommended in assigning the SOGI-PLL parameters. In addition, the design of the loop filter gains becomes difficult since the overall transfer function is of a high order. An enhanced structure SOGI-PLL (ESOGI-PLL) is proposed in [26]. This has a simple design and adequate performance when exposed to high DC offset values. However, the gain of the ESOGI-PLL should be selected carefully so that it does not deteriorate the transient response and harmonic attenuation capability.

Two types of PLLs combining an open-loop frequency-estimator and SOGI block are introduced in [27] using different normalization schemes to remove the dependency of the frequency estimator on grid frequency or phase angle information. The DC offset is canceled using an extra integrator added to the SOGI block to provide accurate grid information estimation with four grid cycles convergence speed. The computation burden of this PLL is reduced using a third-order polynomial approximation to implement the arctangent function, but this comes at the cost of accuracy. Reference [28] discusses many PLLs and FLLs, though most PLLs are either for three-phase systems or based on open-loop PLL structures. The open-loop PLL is beyond the scope of this paper, while because of a lack of signal orthogonality, the design of a single-phase PLL is more challenging than that for three-phase systems.

This paper presents a new method for removing the DC offset effect from a grid synchronization unit using arbitrarily delayed signal cancellation (ADSC) in a SOGI-PLL. A frequency-fixed procedure is adopted to ensure stability and reduced complexity compared with other

SOGI-based PLLs. Unlike other PLLs that rely on a SOGI, the proposed PLL can be accurately represented by a dominant second-order system, making the loop filter design process straightforward. Moreover, the DC offset rejection capability of the proposed method is not restricted to a specific time delay. This gives the proposed PLL more flexibility than other related PLLs. A small-signal model of the proposed PLL is derived for the systematic design of proportional-integral (PI) controller gains. The effects of frequency variations and ADSC on the proposed PLL are considered, and phase and voltage amplitude correction methods are adopted to accurately estimate grid information.

The rest of the paper is organized as follows: Sect. 2 introduces the proposed method, including the required mathematical justifications, the small-signal model, and the PI-controller gain design. Numerical simulations are presented in Sect. 3 to verify and justify the derived small-signal model. Experimental results compared with other related PLLs under different case studies are discussed in Sect. 4, and Sect. 5 concludes the paper.

2 Proposed method

Figure 1 presents the proposed FFSOGI-PLL, which adopts a fixed-frequency concept to reduce implementation complexity, enhance relative stability, and simplify the control design following the recommendations in [14]. As shown in Fig. 1, an ADSC operator is used to cancel the DC offset from the orthogonal signals, v_i is the grid voltage, ω_n is the nominal grid frequency, and $\hat{\omega}_g$ and $\hat{\theta}$ are the estimated grid frequency and phase angle, respectively. τ is the delay length of the ADSC, and k is the SOGI block gain factor. As shown in Fig. 1, the estimated frequency from the SRF-PLL is fed back to the SOGI block to make it frequency adaptive.

The transfer functions of the fixed-frequency SOGI block, as shown in Fig. 1, are:

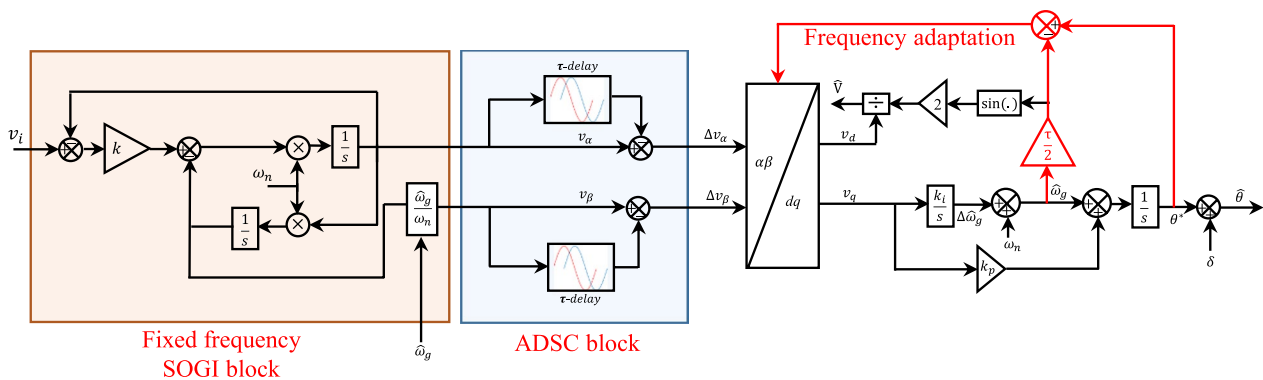


Fig. 1 The proposed FFSOGI-PLL with DC offset rejection capability. The SOGI is used to construct the orthogonality. Arbitrarily delayed signal cancellation is used to remove the DC offset from the orthogonal signals

$$D(s) = \frac{v_\alpha(s)}{v_i(s)} = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \quad (1)$$

$$Q(s) = \frac{v_\beta(s)}{v_i(s)} = \frac{k\omega_n^2}{s^2 + k\omega_n s + \omega_n^2} \quad (2)$$

Assuming a grid voltage of $v_i(t) = V \sin(\omega_g t)$, where V is the voltage amplitude and it is assumed to be 1 pu for simplicity, the Laplace transform for the grid voltage is obtained as:

$$v_i(s) = \frac{\omega_g}{s^2 + \omega_g^2} \quad (3)$$

The output voltage in the s-domain of the SOGI, assuming fixed frequency for a given input voltage, is written as:

$$v_\alpha(s) = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \left(\frac{\omega_g}{s^2 + \omega_g^2} \right) \quad (4)$$

$$v_\beta(s) = \frac{k\omega_n^2}{s^2 + k\omega_n s + \omega_n^2} \left(\frac{\omega_g}{s^2 + \omega_g^2} \right) \quad (5)$$

Simplifying the partial fraction expansion, the time domain $\alpha\beta$ -signals $v_\alpha(t)$ and $v_\beta(t)$ are obtained as:

$$v_\alpha(t) = \frac{k\omega_g \omega_n}{\sqrt{(\omega_n^2 - \omega_g^2)^2 + k^2 \omega_n^2 \omega_g^2}} \sin(\omega_g t - \delta) + A \sin(\omega_d t + \varphi_1) e^{-\frac{k\omega_n}{2} t} \quad (6)$$

$$v_\beta(t) = -\frac{k\omega_n^2}{\sqrt{(\omega_n^2 - \omega_g^2)^2 + k^2 \omega_n^2 \omega_g^2}} \cos(\omega_g t - \delta) + B \cos(\omega_d t + \varphi_2) e^{-\frac{k\omega_n}{2} t} \quad (7)$$

where δ is the phase offset error, $\sin(\delta) = \frac{\omega_g^2 - \omega_n^2}{\sqrt{(\omega_n^2 - \omega_g^2)^2 + k^2 \omega_n^2 \omega_g^2}}$, A , B , φ_1 , φ_2 , and ω_d are functions of ω_g , ω_n , and k .

From (6) and (7), it can be seen that $v_\alpha(t)$ and $v_\beta(t)$ have different amplitudes if $\omega_g \neq \omega_n$. As $|\omega_n^2 - \omega_g^2| \ll k\omega_n \omega_g$, (6) and (7) can be simplified as:

$$v_\alpha(t) = \sin(\omega_g t - \delta) + A \sin(\omega_d t + \varphi_1) e^{-\frac{k\omega_n}{2} t} \quad (8)$$

$$v_\beta(t) = -\frac{\omega_n}{\omega_g} \cos(\omega_g t - \delta) + B \cos(\omega_d t + \varphi_2) e^{-\frac{k\omega_n}{2} t} \quad (9)$$

From (8) and (9), the $v_\alpha(t)$ amplitude is equal to 1, while the $v_\beta(t)$ amplitude is scaled by ω_n/ω_g . The signals after the ADSC operator are given as:

$$\Delta v_\alpha(t) = v_\alpha(t) - v_\alpha(t - \tau) \quad (10)$$

$$\Delta v_\beta(t) = v_\beta(t) - v_\beta(t - \tau) \quad (11)$$

Substituting (8) and (9) into (10) and (11) yields:

$$\begin{aligned} \Delta v_\alpha(t) &= \sin(\omega_g t - \delta) - \sin(\omega_g t - \delta - \omega_g \tau) \\ &\quad + A(\sin(\omega_d t + \varphi_1) - \sin(\omega_d t + \varphi_1 - \omega_d \tau)) e^{-\frac{k\omega_n}{2}(t-\tau)} \\ &= \sin(\omega_g t - \delta) - \sin(\omega_g t - \delta - \omega_g \tau) + D(t) e^{-\frac{k\omega_n}{2} t} \end{aligned} \quad (12)$$

where $D(t) = A(\sin(\omega_d t + \varphi_1) - \sin(\omega_d t + \varphi_1 - \omega_d \tau)) e^{\frac{k\omega_n}{2} \tau}$.

$$\begin{aligned} \Delta v_\beta(t) &= -\cos(\omega_g t - \delta) + \cos(\omega_g t - \delta - \omega_g \tau) \\ &\quad + B(\cos(\omega_d t + \varphi_1) - \cos(\omega_d t + \varphi_1 - \omega_d \tau)) e^{-\frac{k\omega_n}{2}(t-\tau)} \\ &= \cos(\omega_g t - \delta - \omega_g \tau) - \cos(\omega_g t - \delta) + Q(t) e^{-\frac{k\omega_n}{2} t} \end{aligned} \quad (13)$$

where $Q(t) = B(\cos(\omega_d t + \varphi_1) - \cos(\omega_d t + \varphi_1 - \omega_d \tau)) e^{\frac{k\omega_n}{2} \tau}$.

The terms $D(t)$ and $Q(t)$ decay to zero with the time constant $\tau_p = 2/k\omega_n$. Therefore, (12) and (13) are simplified as:

$$\Delta v_\alpha(t) = \sin(\theta - \delta) - \sin(\theta - \delta - \omega_g \tau) \quad (14)$$

$$\Delta v_\beta(t) = -\cos(\theta - \delta) + \cos(\theta - \delta - \omega_g \tau) \quad (15)$$

where $\theta = \omega_g t$. Using a fixed frequency in the SOGI block, $v_\alpha(t)$ is the orthogonal signal to $v_\beta(t) \hat{\omega}_g / \omega_g$ in the frequency-locked state ($\omega_g = \hat{\omega}_g$). Hence, any variation in the grid frequency will result in a small phase difference δ between the actual phase angle θ and that of $v_\alpha(t)$.

If θ^* is the net phase angle difference at the grid side and $\theta^* = \theta - \delta$, the transfer function of the SOGI block can be written as:

$$G_{SOGI}(s) = \frac{\theta^*(s)}{\theta(s)} = \frac{1}{\tau_p s + 1} \quad (16)$$

Equations (14) and (15) can be expressed using θ^* as:

$$\Delta v_\alpha(t) = \sin(\theta^*) - \sin(\theta^* - \omega_g \tau) \quad (17)$$

$$\Delta v_\beta(t) = -\cos(\theta^*) + \cos(\theta^* - \omega_g \tau) \quad (18)$$

Using ADSC to reject the DC offset will cause a phase error, so a phase correction of $\theta_0 = -\frac{\hat{\omega}_g \tau}{2}$ is needed [9, 29]. The $v_q(t)$ signal with the phase correction can be obtained as:

$$v_q(t) = -\sin\left(\hat{\theta} - \frac{\hat{\omega}_g \tau}{2}\right) \Delta v_\alpha(t) + \cos\left(\hat{\theta} - \frac{\hat{\omega}_g \tau}{2}\right) \Delta v_\beta(t) \quad (19)$$

which can be simplified to:

$$v_q(t) = 2\sin\left(\theta^* - \hat{\theta} + \frac{\hat{\omega}_g \tau}{2} - \frac{\omega_g \tau}{2}\right) \sin\left(\frac{\omega_g \tau}{2}\right) \quad (20)$$

2.1 PLL small-signal model

In this section, a small-signal model for the proposed PLL is derived. The term $\sin\left(\frac{\omega_g \tau}{2}\right)$ can be written as:

$$\delta \approx \frac{\omega_n^2 + \Delta\hat{\omega}_g^2 + 2\Delta\hat{\omega}_g\omega_n - \omega_n^2}{k\omega_n(\omega_n + \Delta\hat{\omega}_g)} \approx \frac{\Delta\hat{\omega}_g(\Delta\hat{\omega}_g + 2\omega_n)}{k\omega_n(\omega_n + \Delta\hat{\omega}_g)} \approx \frac{2\Delta\hat{\omega}_g}{k\omega_n} \approx \tau_p \Delta\hat{\omega}_g \quad (28)$$

$$\begin{aligned} \sin\left(\frac{\omega_g \tau}{2}\right) &= \sin\left(\frac{\omega_n \tau}{2}\right) \cos\left(\frac{\Delta\omega_g \tau}{2}\right) \\ &\quad + \cos\left(\frac{\omega_n \tau}{2}\right) \sin\left(\frac{\Delta\omega_g \tau}{2}\right) \end{aligned} \quad (21)$$

In the small-signal analysis, $\cos\left(\frac{\Delta\omega_g \tau}{2}\right) \approx 1$ and $\sin\left(\frac{\Delta\omega_g \tau}{2}\right) \approx \frac{\Delta\omega_g \tau}{2}$. Hence, (21) can be simplified to:

$$\sin\left(\frac{\omega_g \tau}{2}\right) = \sin\left(\frac{\omega_n \tau}{2}\right) + \frac{\Delta\omega_g \tau}{2} \cos\left(\frac{\omega_n \tau}{2}\right) \quad (22)$$

Equation (20) can then be rewritten using (22), as:

$$\begin{aligned} v_q(t) &= 2\sin\left(\theta^* - \hat{\theta} + \frac{\hat{\omega}_g \tau}{2} - \frac{\omega_g \tau}{2}\right) \\ &\quad \left(\sin\left(\frac{\omega_n \tau}{2}\right) + \frac{\Delta\omega_g \tau}{2} \cos\left(\frac{\omega_n \tau}{2}\right)\right) \end{aligned} \quad (23)$$

The term $\Delta\omega_g \tau \left(\Delta\theta^* - \Delta\hat{\theta} + \frac{\Delta\hat{\omega}_g \tau}{2} - \frac{\Delta\omega_g \tau}{2}\right)$ in (23) equals zero in the small-signal analysis, and $v_q(t)$ can be simplified as:

$$v_q(t) = 2\sin\left(\frac{\omega_n \tau}{2}\right) \left(\Delta\theta^* - \Delta\hat{\theta} + \frac{\Delta\hat{\omega}_g \tau}{2} - \frac{\Delta\omega_g \tau}{2}\right) \quad (24)$$

Rearranging (24) yields:

$$v_q(t) = 2\sin\left(\frac{\omega_n \tau}{2}\right) \left(\frac{\Delta\theta^* + \Delta\theta^* - \Delta\omega_g \tau}{2} - \Delta\hat{\theta} + \frac{\Delta\hat{\omega}_g \tau}{2}\right) \quad (25)$$

Applying the Laplace transform to (25) yields:

$$v_q(s) = 2\sin\left(\frac{\omega_n \tau}{2}\right) \left(\frac{1 + e^{-s\tau}}{2} \Delta\theta^*(s) - \Delta\hat{\theta}(s) + \frac{\Delta\hat{\omega}_g(s)\tau}{2}\right) \quad (26)$$

Substituting the value of $\Delta\theta^*(s)$ from (16) into (26) yields:

$$v_q(s) = k_v \left(\frac{1 + e^{-s\tau}}{2} \frac{1}{\tau_p s + 1} \Delta\theta(s) - \Delta\hat{\theta}(s) + \frac{\Delta\hat{\omega}_g(s)\tau}{2}\right) \quad (27)$$

where $k_v = 2\sin\left(\frac{\omega_n \tau}{2}\right)$ is the amplitude scaling factor.

The derived small-signal model does not consider the dynamic of the phase offset error, so to enhance its accuracy, compensation for the phase offset error dynamic is calculated following the guidelines in [1], where $\delta \approx \sin(\delta) \approx \frac{\hat{\omega}_g^2 - \omega_n^2}{k\omega_n\hat{\omega}_g}$. Substituting the values of $\omega_g = \omega_n + \Delta\omega_g$ and $\hat{\omega}_g = \omega_n + \Delta\hat{\omega}_g$, δ can be simplified to:

According to (27) and (28) and based on Fig. 1, the small-signal model of the proposed FFSOGI-PLL is shown in Fig. 2, and the closed-loop transfer function is obtained as:

$$G_{cl}(s) = \frac{\Delta\hat{\theta}_c}{\Delta\theta} = \frac{1}{\tau_p s + 1} \frac{1 + e^{-\tau s}}{2} \frac{k_v(k_p s + k_i)}{s^2 + k_v(k_p - \frac{\tau}{2}k_i)s + k_v k_i} \quad (29)$$

The transfer function in (29) contains a dominant second-order system and a nondominant first-order system. The dominant roots capture the dynamic performance of the system, so the small-signal model can be reduced to a second-order system, as:

$$G_{cl}(s) = \frac{\Delta\hat{\theta}_c}{\Delta\theta} \approx \frac{1 + e^{-\tau s}}{2} \frac{k_v(k_p s + k_i)}{s^2 + k_v(k_p - \frac{\tau}{2}k_i)s + k_v k_i} \quad (30)$$

2.2 PI gains design

From the small-signal model represented by the dominant second-order system as in (30), the following characteristic equation (CE) is obtained:

$s^2 + k_v(k_p - \frac{\tau}{2}k_i)s + k_v k_i = 0$. The second-order system can be designed using linear control theory. The most straightforward method to design the PI-controller gains is to specify the desired damping ratio ζ and the natural damping ω_N of the closed-loop control system. These have a specific desired transient response

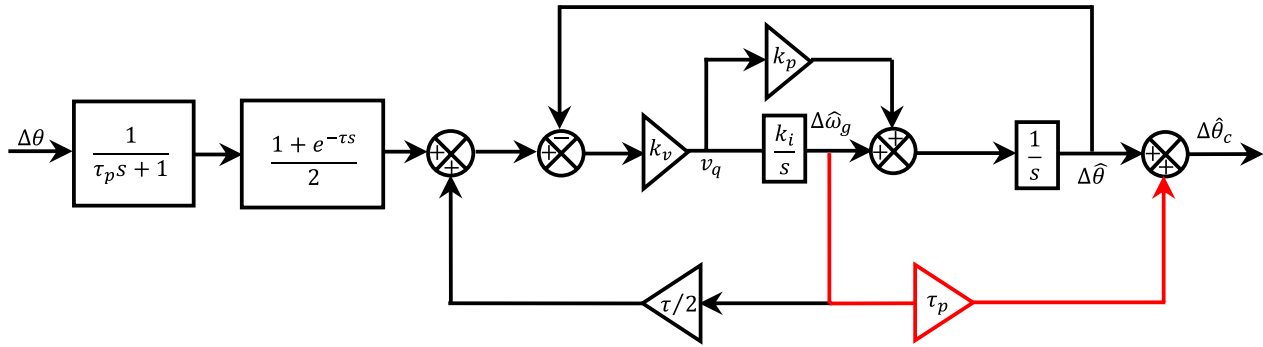


Fig. 2 The small-signal model of the proposed FFSOGI-PLL, where τ is the arbitrary time delay and $\tau_p = 2/k\omega_n$ is the time constant of the SOGI block

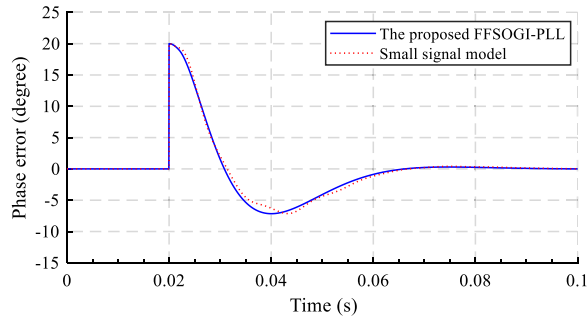


Fig. 3 Performance comparison between the actual response of the proposed FFSOGI-PLL and its small-signal model with a 20° phase jump at 0.02 s

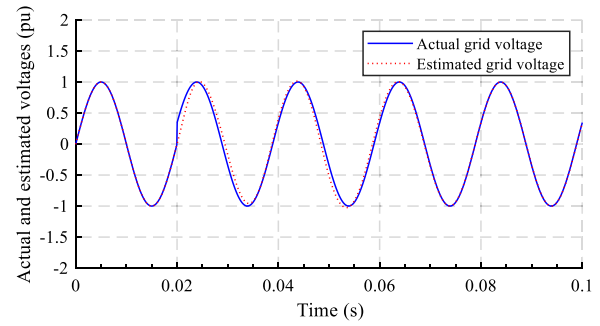


Fig. 4 Actual (solid) and estimated (dashed) grid voltages (pu) under a 20° phase jump at 0.02 s

and bandwidth. Hence, based on ζ and ω_N , the closed-loop CE is obtained as $s^2 + 2\omega_N\zeta s + \omega_N^2 = 0$, and the PI-controller gains are designed by comparing the actual CE with the desired CE. This yields $k_vk_i = \omega_N^2$ and $k_v(k_p - \frac{\tau}{2}k_i) = 2\omega_N\zeta$, from which

$$k_i = \frac{\omega_N^2}{k_v} \quad (31)$$

$$k_p = \frac{2\omega_N\zeta}{k_v} + \frac{\tau k_i}{2} \quad (32)$$

If $\tau = 0.002$ s, $\zeta = 0.707$, and $\omega_N = 41\pi$ rad/s, the PI gains are calculated using (31) and (32) as $k_p = 325.1547$ and $k_i = 27,397$. The SOGI gain factor k should be as large as possible. However, the related PLL small-signal model reveals that a lower value for k leads to better filtering capability but at the cost of a slower dynamic response. Therefore, k should be selected to achieve an acceptable trade-off between the disturbance rejection and response speed. To make a fair comparison with other PLLs, $k = 2$ is selected.

Figure 3 shows the actual and small-signal model responses of the proposed PLL under a phase jump of 20° at 0.02 s, while the actual and estimated voltages are shown in Fig. 4. The results in Figs. 3 and 4 validate the accuracy of the derived small-signal model in predicting the dynamic behavior of the proposed PLL.

The performance of the proposed FFSOGI-PLL is also tested under the following case studies:

Case Study 1: A 20% voltage sag is applied at 0.1 s and recovered to 1 pu at 0.2 s. At 0.3 s, a 20° phase jump occurs, while grid DC voltage offset is imposed at 0.4 s. The grid frequency is fixed at 50 Hz. The results are shown in Fig. 5.

Case Study 2: At 0.1 s, a 3 Hz frequency variation occurs in the grid, while a grid DC voltage offset is added at 0.3 s. The results are shown in Fig. 6.

3 Performance comparisons

The modified SOGI-PLL [4], the modified enhanced PLL (mEPLL) [28], and the ESOGI-FLL [30] are compared with the proposed PLL. There is a coupling term between the SOGI block and SRF-PLL [4, 7, 31]. Hence,

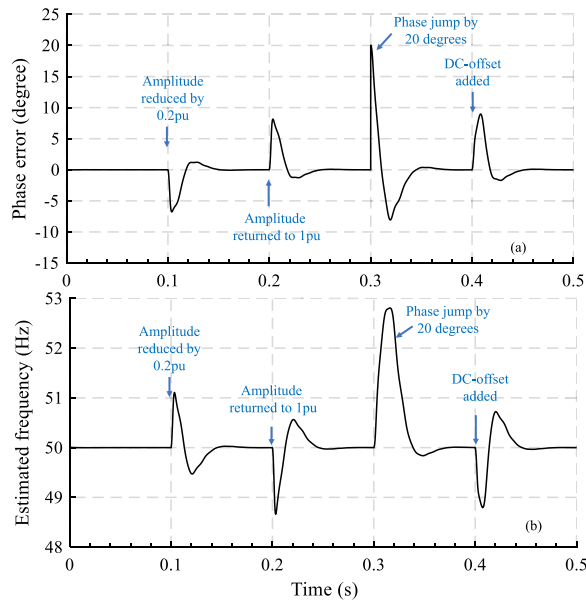


Fig. 5 Results of case study 1 grid conditions. **a** Estimated phase error and **b** estimated grid frequency

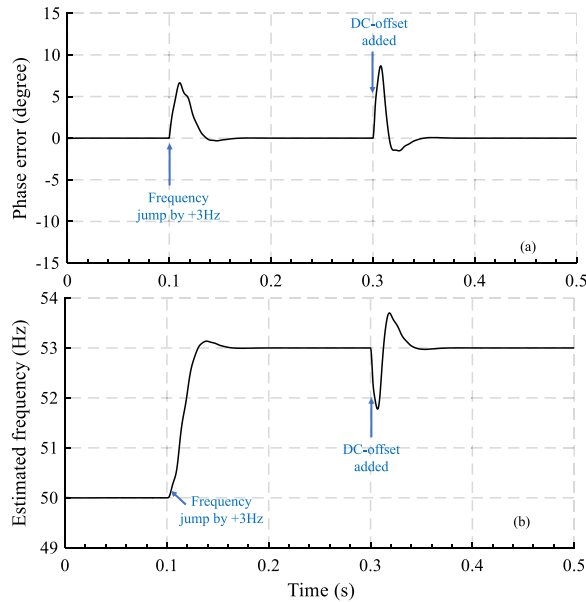


Fig. 6 Results of case study 2 grid conditions. **a** Estimated phase error and **b** estimated grid frequency

the gain selection of the SOGI block k can affect the system's stability. Therefore, for a fair comparison with the other SOGI-PLLs, the gain of the SOGI block needs to be as large as possible to achieve a fast dynamic response. Thus, the gain of the SOGI block is set to 2 for all PLLs, including the proposed one.

The PI-controller gains for the modified SOGI-PLL are determined based on the symmetrical optimum method because it has a third-order transfer function [4, 31, 32]. In the symmetrical optimum method [33], if the crossover frequency ω_c is made equal to the natural frequency ω_N , the following parameters are defined:

$$\begin{cases} k_p = \omega_c \\ k_i = \omega_c^2 / b \\ \omega_p = b\omega_c \\ \tau_p = 1/\omega_p \\ k = 2/\tau_p\omega_n \end{cases} \quad (33)$$

where b is a constant that determines the phase margin (PM) and the system stability as:

$$PM = \tan^{-1}\left(\frac{b^2 - 1}{2b}\right) \quad (34)$$

For the recommended PM of $30^\circ < PM < 60^\circ$, b is selected to be $1 + \sqrt{2}$ by considering a damping factor ζ of 0.707 and PM of 45° , in order to guarantee sufficient system robustness and a fair comparison with the proposed PLL. In addition, ω_N is selected as 41π rad/s for all the PLLs. Hence, based on (33) and (34), the PI-controller gains for the modified SOGI-PLL are $k_p = 130.129$ and $k_i = 70,141$.

The PI gains for the mEPLL and ESOGI-PLL are adopted to be the same as the proposed PLL for the purpose of a fair comparison. They are $k_p = 325.1547$ and $k_i = 27,397$.

The following case studies are considered for the comparisons:

Case 1: A phase jump of 20° at 0.04 s, and the results are shown in Fig. 7.

Case 2: A phase jump of 20° and DC offset of 0.15 pu are added to the grid voltage at 0.04 s. The results are shown in Fig. 8.

Case 3: The grid frequency is changed from 50 to 53 Hz at 0.04 s, and the results are shown in Fig. 9.

Case 4: The grid frequency is changed from 50 to 53 Hz, and a DC offset of 0.15 pu is added to the grid voltage at 0.04 s. The results are shown in Fig. 10.

Case 5: A 0.15 pu DC offset is added to the grid voltage at 0.04 s, and the results are shown in Fig. 11.

Case 6: A 0.2 pu voltage sag and a 0.15 pu DC offset are added to the grid voltage at 0.04 s. The results are shown in Fig. 12.

Several comparative simulations are carried out using MATLAB/Simulink to test the dynamic performance under a 20° phase jump and 3 Hz frequency drift with and without a DC offset. The results are shown in Figs. 7–10 and are summarized in Table 1. The settling time of the proposed PLL is faster than the other PLLs

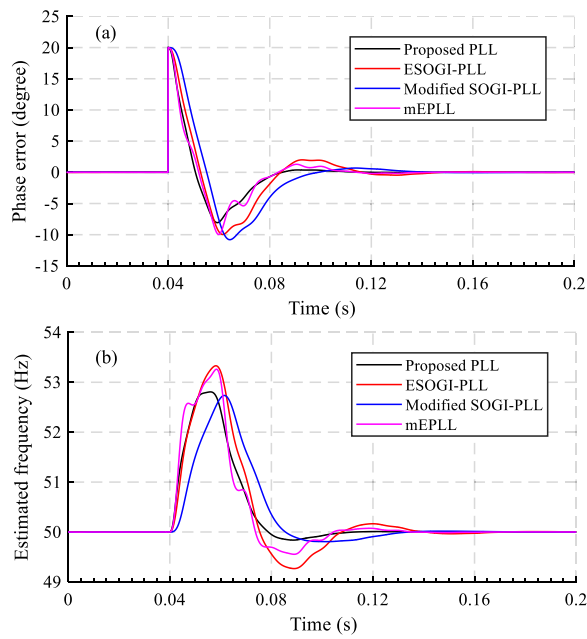


Fig. 7 Performance comparison between the proposed PLL, ESOGI-PLL, modified SOGI-PLL, and mEPLL under Case 1 (a phase jump of 20° at 0.04 s). **a** Estimated phase error and **b** estimated grid frequency

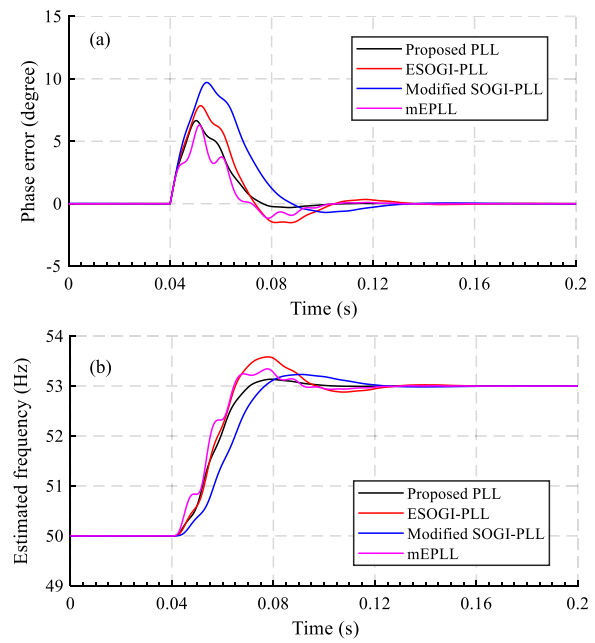


Fig. 9 Performance comparison between the proposed PLL, ESOGI-PLL, modified SOGI-PLL, and mEPLL under Case 3 (a frequency jump by 3 Hz at 0.04 s). **a** Estimated phase error and **b** estimated grid frequency

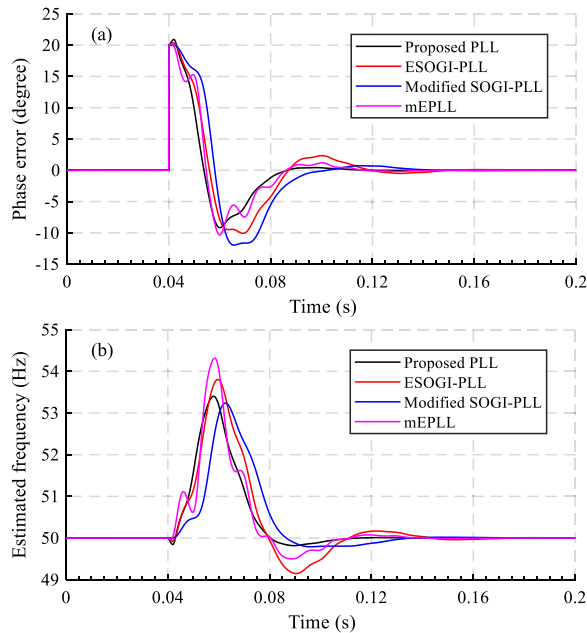


Fig. 8 Performance comparison between the proposed PLL, ESOGI-PLL, modified SOGI-PLL, and mEPLL under Case 2 (a phase jump of 20° and a DC offset of 0.15 pu added to the grid voltage at 0.04 s). **a** Estimated phase error and **b** estimated grid frequency

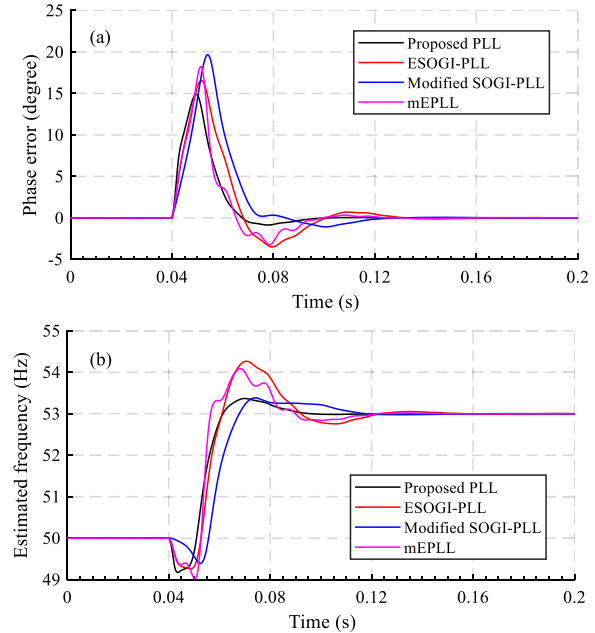


Fig. 10 Performance comparison between the proposed PLL, ESOGI-PLL, modified SOGI-PLL, and mEPLL under Case 4 (a frequency jump of 3 Hz and a DC offset of 0.15 pu added to the grid voltage at 0.04 s). **a** Estimated phase error and **b** estimated grid frequency

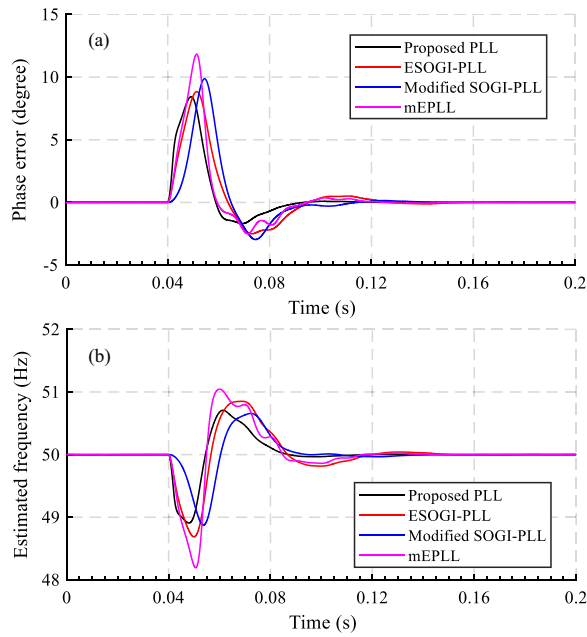


Fig. 11 Performance comparison between the proposed PLL, ESOGI-PLL, modified SOGI-PLL, and mEPLL under Case 5 (a 0.15 pu DC offset added to the grid voltage at 0.04 s). **a** Estimated phase error and **b** estimated grid frequency

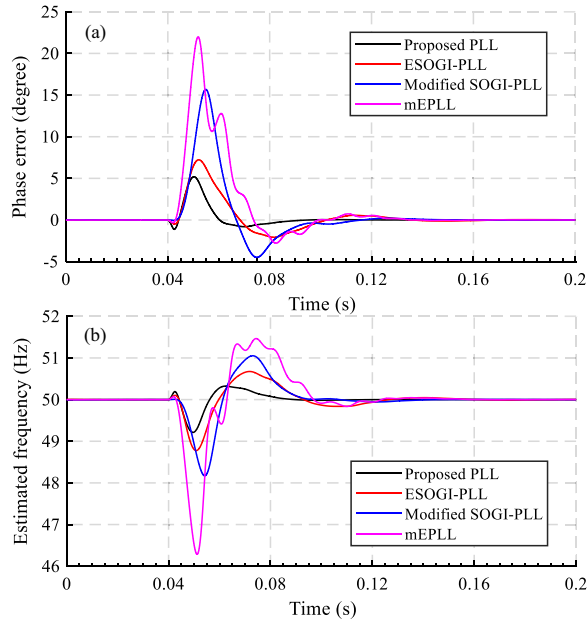


Fig. 12 Performance comparison between the proposed PLL, ESOGI-PLL, modified SOGI-PLL, and mEPLL under Case 6 (grid voltage amplitude reduced by 0.2 pu with a 0.15 pu DC offset added to the grid voltage at 0.04 s). **a** Estimated phase error and **b** estimated grid frequency

by around two grid cycles, as seen in Figs. 7–10. The settling times of the modified SOGI-PLL and ESOGI-PLL are about four grid cycles under the phase and frequency jump with and without a DC offset, which is twice the proposed PLL. The mEPLL converges within three grid cycles. In addition, the proposed PLL has less phase overshoot than the other PLLs, while the estimated peak frequency is almost the same for all the PLLs.

The DC offset rejection performance of the proposed PLL compared with the other PLLs is depicted in Fig. 11. The settling time of the proposed PLL is around two grid cycles,

which is slightly faster than the mEPLL and the modified SOGI-PLL. The settling time for the ESOGI-PLL is about three grid cycles. However, the peak frequency deviation and peak phase error of the proposed PLL are less than the other PLLs.

Under the effect of the combined voltage sag and DC offset, the proposed PLL's settling time is around two grid cycles, which is much faster than the other PLLs. The peak phase and frequency errors are also less than the other PLLs, as shown in Fig. 12.

Overall, the proposed PLL has the fastest transient response and better dynamic performance than the other PLLs for almost all the performance indices listed in Table 1, hence offering an improved solution for precise grid synchronization in single-phase applications.

4 Experimental results

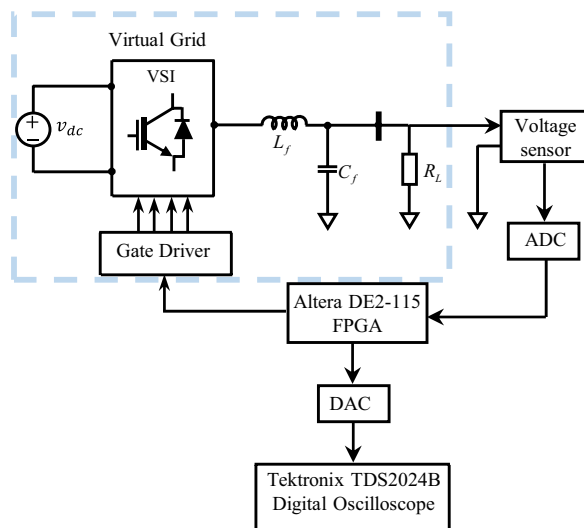
Here, the theoretical findings of the proposed PLL are experimentally verified, with comparisons made to the mEPLL and modified SOGI-PLL. The small-scale set-up, which consists of a voltage source inverter (VSI) connected to an R load via an LC filter to form a virtual grid, is shown in Fig. 13.

The VSI is controlled in an open-loop to mimic the occurrence of different cases, such as phase jump, frequency variation, voltage sag, and DC offset. The point of common coupling is measured using an LV25-P voltage sensor, and an offset and scaling circuit is used to shape the grid voltage to make it suitable for the analog-to-digital converter (ADC) module.

The experimental data are processed by an Altera DE2-115 field-programmable gate array (FPGA) board, and a Tektronix TDS2024B digital oscilloscope is used to observe the digital-to-analog converter (DAC) module results. The VSI switching frequency is 10 kHz, the filter has the values of $L_f = 0.1$ mH and $C_f = 10$ μ F, and the nominal grid frequency is 50 Hz. For the experimental validation, the arbitrary time delay τ of the proposed PLL is set

Table 1 Summarized results for the different PLLs and the proposed PLL

Case study	Proposed FFSOGI-PLL	ESOGI-PLL	Modified SOGI-PLL	mEPLL
<i>20° phase jump</i>				
2% phase settling time (ms)	41.60	92.90	86.30	64.50
Phase overshoot (%)	40.3835	49.81	54.01	49.84
Peak frequency (Hz)	52.81	53.33	52.74	53.26
<i>20° phase jump and 0.15 pu DC offset</i>				
2% phase settling time (ms)	42.40	95.30	89.10	71.30
Phase overshoot (%)	45.89	50.41	59.78	51.77
Peak frequency (Hz)	53.40	53.80	53.24	54.31
<i>3 Hz frequency jump</i>				
2% frequency settling time (ms)	47.80	79.40	74.00	64.7
Frequency overshoot (%)	0.26	1.10	0.44	0.65
Peak phase error (°)	6.65	7.85	9.71	6.31
Peak frequency (Hz)	53.10	53.58	53.23	53.34
<i>3 Hz frequency jump and 0.15 pu DC offset</i>				
2% frequency settling time (ms)	48.20	78.30	69.90	71.10
Frequency overshoot (%)	0.69	2.39	0.72	2.05
Peak phase error (°)	14.91	16.55	19.67	18.23
Peak frequency (Hz)	53.37	54.27	53.38	54.09
<i>0.15 pu DC offset only</i>				
2% phase settling time (ms)	43.60	74.70	50.10	47.50
Absolute peak phase error (°)	8.43	8.84	9.87	11.83
Peak frequency deviation (Hz)	1.09	1.29	1.12	1.81
<i>Amplitude reduced by 0.2 pu and 0.15 pu DC offset</i>				
2% phase settling time (ms)	40.30	83.40	66.60	82.50
Peak phase error (°)	5.19	7.23	15.68	21.99
Peak frequency deviation (Hz)	0.79	1.22	1.82	3.70

**Fig. 13** The block diagram of the small-scale experimental set-up

to 0.005 s. This results in the PI-controller gains of $k_p = 158.134$ and $k_i = 11,731$.

The estimated phase error and frequency results under a 20° phase jump are shown in Fig. 14. The results of the 3 Hz frequency drift are shown in Fig. 15. Figure 16 shows the results under a voltage sag of 0.2 pu. Finally, the results under a DC offset of 0.15 pu are shown in Fig. 17. The results show that the proposed PLL converges faster than the other PLLs and has a better dynamic performance.

It should be noted that the harmonic test is considered indirectly for all the experimental tests. The VSI with pulse width modulation and cascaded with the LC filter is a source of harmonics; the total harmonic distortion in the sensed grid voltage is 11.69%.

The experimental results verified the simulations. This validates the applicability of the proposed PLL as an improved synchronization technique for single-phase applications.

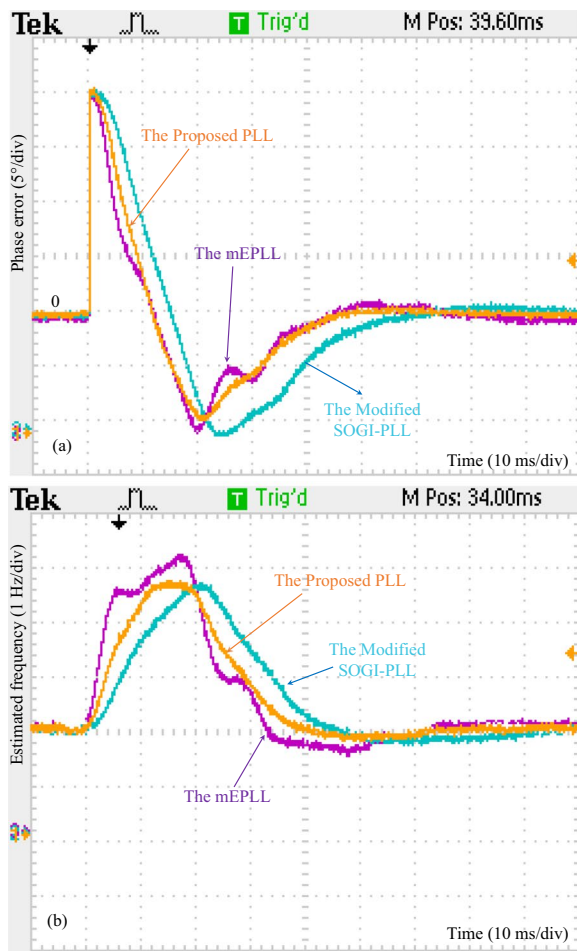


Fig. 14 Experimental results under a 20° phase jump. CH1, CH2, and CH3 show the responses of the proposed PLL, mEPLL, and modified SOGI-PLL, respectively. **a** Estimated phase error and **b** estimated grid frequency

5 Conclusion

In this paper, a new DC offset rejection method using an ADSC operator has been proposed for grid-connected converters in single-phase applications that is not limited to a specific time delay. The proposed PLL adopts a fixed-frequency SOGI to decrease the implementation complexity, enhance relative stability, and simplify the control design. Although other PLLs rely on a specified delay value to reject DC offset, the proposed method is not restricted to a specific time delay. Moreover, unlike other PLLs that rely on a SOGI, the proposed PLL can be accurately represented by a dominant second-order

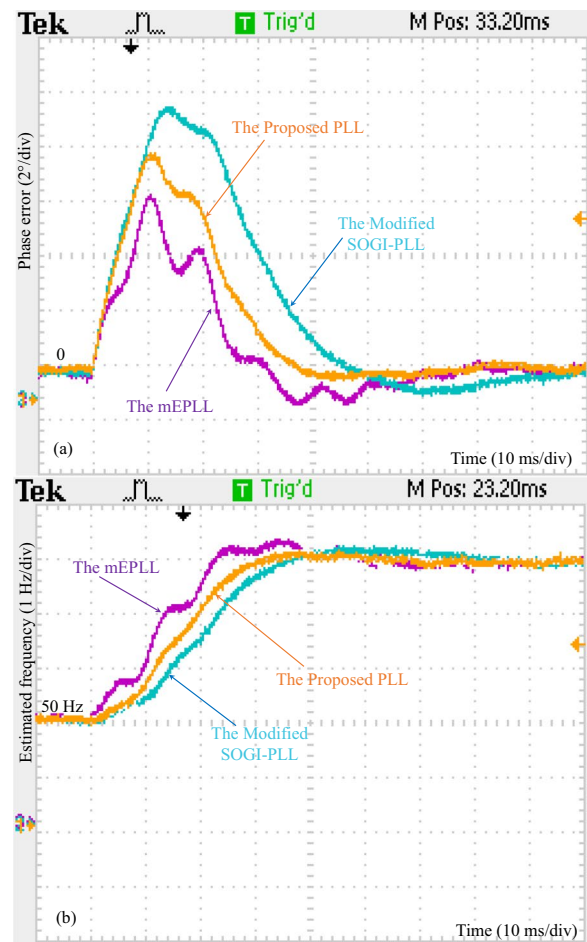


Fig. 15 Experimental results under a sudden change of 3 Hz grid frequency. CH1, CH2, and CH3 show the responses of the proposed PLL, mEPLL, and modified SOGI-PLL, respectively. **a** Estimated phase error and **b** estimated grid frequency

system, which simplifies the controller design. The statistical results of the numerical simulations under different cases, such as phase jump, frequency variation, voltage sag, and DC offset, show that the proposed PLL has the fastest transient response and better dynamic performance than other PLLs on almost all performance indices. The performance of the proposed PLL is experimentally validated and compared with the analytical results. They show a better dynamic performance than other PLLs. Therefore, the proposed PLL offers an improved solution for precise grid synchronization.

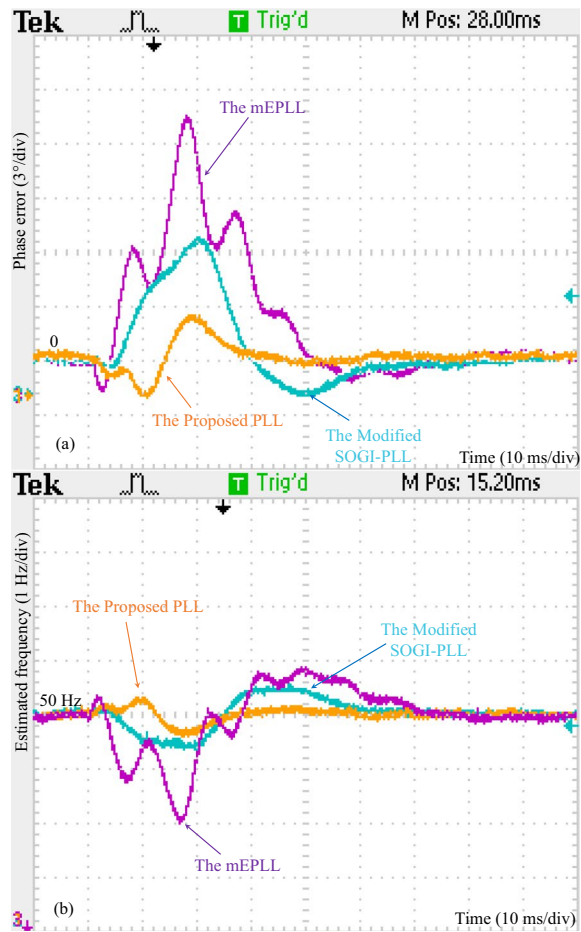


Fig. 16 Experimental results under a 20% voltage sag. CH1, CH2, and CH3 the proposed PLL, mEPLL, and modified SOGI-PLL, respectively. **a** Estimated phase error and **b** estimated grid frequency

Abbreviations

ADSC: Arbitrarily Delayed Signal Cancellation; ADC: Analog-to-Digital Converter; CE: Characteristic Equation; CGI: Cascaded Generalized Integrator; DAC: digital-to-analog-converter; ESOGI-PLL: Enhanced structure SOGI-PLL; FFSOGI-PLL: Frequency-Fixed SOGI-based PLL; FLL: Frequency-Locked Loop; FPGA: Field-Programmable Gate Array; mEPLL: Modified Enhanced PLL; MSTOGI: Mixed Second and Third-Order Generalized Integrator; OSG: Orthogonal Signal Generation; PCC: The Point of Common Coupling; PI: Proportional-Integral; PM: The Phase Margin; PLL: Phase-Locked Loop; SOGI: Second-Order Generalized Integrator; SRF-PLL: Synchronous Reference Frame-based PLL; THD: Total Harmonic Distortion; TOGI: Third-Order Generalized Integrator.

List of symbols

A, B, φ, φ_2 and ω_d : Variables function of ω_g, ω_n , and k ; b : The constant that determines the phase margin; $D(t)$ & $Q(t)$: Terms decaying to zero at time constant equal τ_p ; δ : The phase offset error; $\Delta\omega_g$: The deviation of the grid frequency from its nominal value; $\Delta\hat{\omega}_g$: The deviation in estimated grid frequency; $\Delta\theta^*$: The deviation in the estimated value of the phase error compensator; $\Delta\hat{\theta}$: The deviation in the estimated phase; $\Delta\theta$: The deviation in the grid voltage phase; $\Delta v_{\alpha\beta}(t)$: The signals after the ADSC operator; k : The SOGI block's gain factor; k_v : The amplitude scaling factor; k_p : The proportional gain of the PI-controller; k_i : The integral gain of the PI-controller; τ : The delay length of the ADSC; τ_p : The time constant of FFSOGI-PLL; θ : Grid voltage phase; $\hat{\theta}$: The estimated phase; θ^* : The net phase angle difference at the grid side; V : The grid amplitude; $v_{\alpha}(t)$ & $v_{\beta}(t)$: The time-domain $\alpha\beta$ -signals; v_i : The grid voltage; ω_n : The nominal grid frequency; ω_g : The actual grid frequency; $\hat{\omega}_g$: The estimated grid frequency; ω_n :

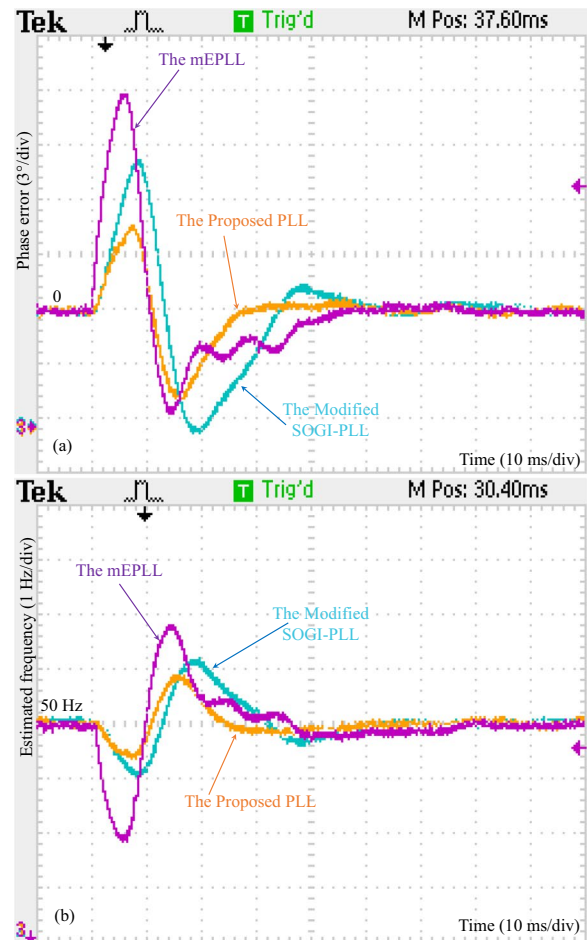


Fig. 17 Experimental results under a 0.15 pu DC offset. CH1, CH2, and CH3 show the responses of the proposed PLL, mEPLL, and modified SOGI-PLL, respectively. **a** Estimated phase error and **b** estimated grid frequency

The natural frequency; ω_c : The crossover frequency; ξ : The desired damping ratio.

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Authors' contributions

Issam A. Smadi proposed the research idea formulations and built the experimental set-up. All authors participated in formulating the control design and in implementing it. Bayan H. Bany Fawaz was in charge of running different simulations and writing the first draft of the paper. Issam A. Smadi updated the literature review and improved the quality of the presentation. All authors participated in verifying the results and providing answers to all comments from reviewers. All authors read and approved the final manuscript.

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Availability of data and materials

All data generated or analyzed during this study are included in the published article.

Declarations

Competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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References

- Golestan, S., Mousazadeh, S. Y., Guerrero, J. M., & Vasquez, J. C. (2017). A critical examination of frequency-fixed second-order generalized integrator-based phase-locked loops. *IEEE Transactions on Power Electronics*, 32(9), 6666–6672. <https://doi.org/10.1109/TPEL.2017.2674973>
- Mohamadian, S., Pairo, H., & Ghasemian, A. (2021). A straightforward quadrature signal generator for single-phase SOGI-PLL with low susceptibility to grid harmonics. *IEEE Transactions on Industrial Electronics*. <https://doi.org/10.1109/TIE.2021.3095813>
- Zhang, C., Zhao, X., Wang, X., Chai, X., Zhang, Z., & Guo, X. (2018). A grid synchronization PLL method based on mixed second-and third-order generalized integrator for DC offset elimination and frequency adaptability. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 6(3), 1517–1522. <https://doi.org/10.1109/JESTPE.2018.2810499>
- Xie, M., Wen, H., Zhu, C., & Yang, Y. (2017). DC offset rejection improvement in single-phase SOGI-PLL algorithms: Methods review and experimental evaluation. *IEEE Access*, 5, 12810–12819. <https://doi.org/10.1109/ACCESS.2017.2719721>
- Lubura, S., Šoja, M., Lale, S. A., & Ikić, M. (2014). Single-phase phase locked loop with DC offset and noise rejection for photovoltaic inverters. *IET Power Electronics*, 7(9), 2288–2299. <https://doi.org/10.1049/iet-pel.2013.0413>
- Kulkarni, A., & John, V. (2017). Design of a fast response time single-phase PLL with DC offset rejection capability. *Electric Power Systems Research*, 145, 35–43. <https://doi.org/10.1016/j.epsr.2016.12.023>
- Golestan, S., Guerrero, J. M., & Vasquez, J. C. (2017). Single-phase PLLs: A review of recent advances. *IEEE Transactions on Power Electronics*, 32(12), 9013–9030. <https://doi.org/10.1109/TPEL.2017.2653861>
- Dai, Z., Zhao, P., Chen, X., Fan, M., & Zhang, J. (2019). An enhanced transfer delay-based frequency locked loop for three-phase systems with DC offsets. *IEEE Access*, 7, 40380–40387. <https://doi.org/10.1109/ACCESS.2019.2903581>
- Smadi, I. A., & Fawaz, B. H. B. (2021). Phase-locked loop with DC offset removal for single-phase grid-connected converters. *Electric Power Systems Research*, 194, 106980. <https://doi.org/10.1016/j.epsr.2020.106980>
- Golestan, S., Guerrero, J. M., Vasquez, J. C., Abusorrah, A. M., & Al-Turki, Y. (2018). Advanced single-phase DSC-based PLLs. *IEEE Transactions on Power Electronics*, 34(4), 3226–3238. <https://doi.org/10.1109/TPEL.2018.2856931>
- Gude, S., & Chu, C. C. (2019). Dynamic performance enhancement of single-phase and two-phase enhanced phase-locked loops by using in-loop multiple delayed signal cancellation filters. *IEEE Transactions on Industry Applications*, 56(1), 740–751. <https://doi.org/10.1109/TIA.2019.2943556>
- Stojić, D. (2021). Improved observer-based quadrature signal generator. *Electrical Engineering*. <https://doi.org/10.1007/s00202-021-01294-6>
- Ahmed, H., Biricik, S., & Benbouzid, M. (2020). Low-pass filtering or gain tuning free simple dc offset rejection technique for single and three-phase systems. *Electric Power Systems Research*, 186, 106422. <https://doi.org/10.1016/j.epsr.2020.106422>
- Xiao, F., Dong, L., Li, L., & Liao, X. (2016). A frequency-fixed SOGI-based PLL for single-phase grid-connected converters. *IEEE Transactions on Power Electronics*, 32(3), 1713–1719. <https://doi.org/10.1109/TPEL.2016.2606623>
- Hui, N., Wang, D., & Li, Y. (2018). A novel hybrid filter-based PLL to eliminate effect of input harmonics and DC offset. *IEEE Access*, 6, 19762–19773. <https://doi.org/10.1109/ACCESS.2018.2821704>
- Pal, K., Naqvi, S. B. Q., Singh, B., & Kandpal, T. C. (2020). MMLSTOGI based control for suppression of current harmonics in PV-tied grid. *IET Power Electronics*, 13(16), 3697–3706. <https://doi.org/10.1049/ietpel.2020.0087>
- Prakash, S., Singh, J. K., Behera, R. K., & Mondal, A. (2019). Comprehensive analysis of SOGI-PLL based algorithms for single-phase system. In *2019 national power electronics conference (NPEC)* (pp. 1–6). IEEE. <https://doi.org/10.1109/NPEC47332.2019.9034724>
- Dao, T., Biricik, S., & Ngo, T. (2020). A comprehensive analysis of grid synchronization systems for power converters. In *IECON 2020 The 46th annual conference of the IEEE industrial electronics society* (pp. 4935–4940). IEEE. <https://doi.org/10.1109/IECON43393.2020.9255348>
- Saxena, H., Singh, A., & Rai, J. N. (2021). Enhanced third-order generalized integrator-based grid synchronization technique for DC-offset rejection and precise frequency estimation. *Arabian Journal for Science and Engineering*. <https://doi.org/10.1007/s13369-021-05559-x>
- Xu, J., Qian, H., Hu, Y., Bian, S., & Xie, S. (2021). Overview of SOGI-based single-phase phase-locked loops for grid synchronization under complex grid conditions. *IEEE Access*, 9, 39275–39291. <https://doi.org/10.1109/ACCESS.2021.3063774>
- Bamigbade, A., Khadkikar, V., & Al Hosani, M. (2020). Single-phase type-1 frequency-fixed pll for distorted voltage condition. *IEEE Transactions on Industrial Electronics*, 68(5), 3865–3875. <https://doi.org/10.1109/TIE.2020.2984999>
- Akhtar, M. A., & Saha, S. (2019). An adaptive frequency-fixed second-order generalized integrator-quadrature signal generator using fractional-order conformal mapping based approach. *IEEE Transactions on Power Electronics*, 35(6), 5548–5552. <https://doi.org/10.1109/TPEL.2019.2951427>
- Yu, J., Shi, W., Li, J., Deng, L., & Pei, M. (2020). A discrete-time non-adaptive SOGI-based frequency-locked loop. *IEEE Transactions on Power Systems*, 35(6), 4912–4915. <https://doi.org/10.1109/TPWRS.2020.3018625>
- Bamigbade, A., Khadkikar, V., & Al Hosani, M. (2020). A type-3 PLL for single-phase applications. *IEEE Transactions on Industry Applications*, 56(5), 5533–5542. <https://doi.org/10.1109/TIA.2020.2999435>
- Prakash, S., Singh, J. K., Behera, R. K., & Mondal, A. (2021). A type-3 modified SOGI-PLL with grid disturbance rejection capability for single-phase grid-tied converters. *IEEE Transactions on Industry Applications*. <https://doi.org/10.1109/TIA.2021.3079122>
- Kherbachi, A., Chouder, A., Bendib, A., Kara, K., & Barkat, S. (2019). Enhanced structure of second-order generalized integrator frequency-locked loop suitable for DC-offset rejection in single-phase systems. *Electric Power Systems Research*, 170, 348–357. <https://doi.org/10.1016/j.epsr.2019.01.029>
- Sahoo, A., Ravishankar, J., & Jones, C. (2021). Phase-locked loop independent second-order generalized integrator for single-phase grid synchronization. *IEEE Transactions on Instrumentation and Measurement*, 70, 1–9. <https://doi.org/10.1109/TIM.2021.3104406>
- Golestan, S., Guerrero, J. M., Vasquez, J. C., Abusorrah, A. M., & Al-Turki, Y. (2020). Linear time-periodic modeling, examination, and performance enhancement of grid synchronization systems with DC component rejection/estimation capability. *IEEE Transactions on Power Electronics*, 36(4), 4237–4253. <https://doi.org/10.1109/TPEL.2020.3018584>
- Smadi, I. A., & Issa, M. B. (2019). Phase locked loop with DC-offset removal for grid synchronization. In *IECON 2019–45th annual conference of the IEEE industrial electronics society* (Vol. 1, pp. 4669–4673). IEEE. <https://doi.org/10.1109/IECON.2019.8926845>
- Du, H., Sun, Q., Cheng, Q., Ma, D., & Wang, X. (2019). An adaptive frequency phase-locked loop based on a third order generalized integrator. *Energies*, 12(2), 309. <https://doi.org/10.3390/en12020309>
- Karimi-Ghartemani, M., Khajehoddin, S. A., Jain, P. K., Bakhshai, A., & Mojiri, M. (2011). Addressing DC component in PLL and notch filter algorithms. *IEEE Transactions on Power Electronics*, 27(1), 78–86. <https://doi.org/10.1109/TPEL.2011.2158238>
- Golestan, S., Monfared, M., & Guerrero, J. M. (2013, February). Second order generalized integrator based reference current generation method for single-phase shunt active power filters under adverse grid conditions. In *4th Annual International Power Electronics, Drive Systems and Technologies Conference* (pp. 510–517). IEEE. <https://doi.org/10.1109/PEDSTC.2013.6506761>
- Golestan, S., Monfared, M., Freijedo, F. D., & Guerrero, J. M. (2012). Design and tuning of a modified power-based PLL for single-phase grid-connected power conditioning systems. *IEEE Transactions on Power Electronics*, 27(8), 3639–3650. <https://doi.org/10.1109/TPEL.2012.2183894>