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A novel complex current ratio-based technique for transmission line protection



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Abstract

With respect to sensitivity, selectivity and speed of operation, the current differential scheme is a better way to protect transmission lines than overcurrent and distance-based schemes. However, the protection scheme can be severely influenced by the Line Charging Capacitive Current (LCCC) with increased voltage level and Current Transformer (CT) saturation under external close-in faults. This paper presents a new UHV/EHV current-based protection scheme using the ratio of phasor summation of the two-end currents to the local end current, instead of summation of the two-end currents, to discriminate the internal faults. The accuracy and effectiveness of the proposed protection technique are tested on the 110 kV Western System Coordinating Council (WSCC) 9-bus system using PSCAD/MATLAB. The simulation results confirm the reliable operation of the proposed scheme during internal/external faults and its independence from fault location, fault resistance, type of fault, and variations in source impedance. Finally, the effectiveness of the proposed scheme is also verified with faults during power swing and in series compensated lines.

Keywords: Current differential protection, Line charging capacitive current, CT saturation, Fault discrimination, Phasor summation of currents

1 Introduction

To accommodate increased load demand and the need for transmitting large amounts of power over long distances, high volta ge long transmission lines play a large role in the operation of a power system. However, protection of these lines is a challenging task for engineers, where multiple system parameters are involved. Generally, distance protection schemes are used for such lines. These provide satisfactory results but also come with certain drawbacks, such as sensitivity to fault resistance and infeed current from remote sources, etc. [1]. Hence, in view of selectivity, sensitivity, and speed of operation, a pilot wire differential protection scheme is preferred to distance-based and overcurrent approaches because of its high sensitivity with crisp demarcation of the protective zone [2]. Furthermore, this method improves the speed of operation and can provide favorable performance during power swings and external faults [3].

However, it has limited application because of signal attenuation caused by the series resistance and shunt capacitance of the pilot wires. Some of the issues have been nullified by the infiltration of modern optical communication technology, which helps to transfer real-time synchronized data at high speed [4]. However, when working on Ultra-High Voltage (UHV) and Extra-High Voltage (EHV) transmission lines, the conventional current differential scheme has limited performance because of: (i) Line Charging Capacitive Current (LCCC) [5], and (ii) Current Transformer (CT) saturation during close-in external faults [6].

1.1 Effect of LCCC

The basic differential scheme relies on the summation of all currents in the respective zone of protection. Ideally, this summation is zero for all events except internal faults. However, in case of a practical long transmission line, this sum is not zero because of the presence of LCCC and data measurements. For instance, it is recognized in the literature that high-voltage overhead lines draw about 1 A charging current per kilometer and in

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some extreme cases this current can even be comparable to a high resistive fault current [7]. Hence, this charging current can result in mal-operation of the relay even in normal operating conditions. Therefore, to mitigate the LCCC effect, various compensation techniques have been proposed.

In [8], transient distributed line capacitive current is used as a compensation parameter. However, it is only effective during steady state but not for transient capacitive current. In [9], a phase-let-based differential scheme with transient capacitive current compensation is proposed. This scheme thoroughly examines the dynamic behavior of the differential relays to improve their performance. However, these methods [9, 10] require detailed transmission line parameters which may not be available in practice.

Using the theory of Equal Transfer Process of Transmission Lines (ETPTL), an instantaneous value-based differential protection scheme is proposed in [11]. The method calculates the instantaneous value of the capacitive current which is then removed before implementing the differential criterion. Hence, this scheme requires voltage data along with current data.

1.2 Effect of CT Saturation

CT is one of the important devices in the protection of electrical equipment, and its characteristics will have a significant impact on the performance of the differential scheme. CT saturation causes distortion of the current signal wave shape which can result in mal-operation of the relay. To overcome this, reference [12] proposes a scheme based on symmetrical components, while a scheme for CT saturation detection based on the measurement of source impedance at the relay location is elaborated in [13]. In addition, adaptive-based differential schemes are proposed in [14, 15] to enhance the security of the relay against external faults during CT saturation. Nevertheless, the impact of CT saturation has not been eliminated and consequently, it still compromises the achievement of sufficient security.

Fast Traveling-Wave (TW) based differential protection schemes are proposed in [16, 17]. However, these methods require high-speed processors to implement the proposed scheme for better operation. This is not economically feasible. An adaptive current differential method [18] is presented. This enhances the sensitivity and speed of operation of the conventional differential scheme without jeopardizing its security. However, the accuracy of this technique relies on the assumption that the measured data is synchronized.

To improve the authenticity of the relay during such conditions, an Alpha (α)-Plane relaying scheme is implemented in most line protections [19, 20], where the current ratio of the two ends is used to distinguish the internal faults. Here, the phase current-based Alpha (α)-Plane relaying has a

large restraining region to facilitate high immunity to CT saturation, LCCC, and errors in data synchronization. In addition, a sequence current-based scheme has enhanced performance during conditions of high fault resistance [21]. In [22], both sequence and phase currents are used to revamp the sensitivity of the Alpha (α)-Plane scheme to provide better reliability under various power system operating conditions. Typically, this scheme incorporates a total of 5 characteristics to provide complete protection of lines under all types of shunt faults, including 3 phase elements (87LA, 87LB, 87LC), and 2 sequence elements (87LG and 87 L2) of the zero and negative sequences [21-23]. However, the focus is on developing an effective differential scheme based on the ratio of phasor summation of the two-end currents to the local end current, instead of the summation of the two-end currents. In this paper, the complete protection of the line is fulfilled by only phase current characteristics and does not require negative and zero sequence characteristics. The validation of the proposed method is examined through the 110-kV WSCC 9bus system using EMTDC/PSCAD and MATLAB tools.

The remainder of this paper is organized as follows. Section II provides the definition of the proposed scheme and section III describes the setting procedure of the restraining region. Simulation results and discussion are given in Section IV. The proposed scheme is tested under various operating conditions in Section V and a comparative assessment is given in Section VI. Finally, the conclusion is drawn in Section VII.

2 Definition of the proposed scheme

To design and analyze the performance of the proposed scheme, a doubly-fed transmission system is considered as shown in Fig. 1 and the respective notations are given in Table 1. For the proposed scheme, the locus of Complex Current Ratio (*CCR*) is defined as:

$$CCR = \frac{\tilde{I}_{Sum}}{\tilde{I}_{Bus}} \tag{1}$$

where I_{Bus} is the current measured at the locus bus.

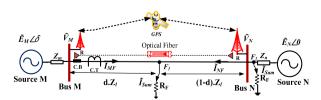


Fig. 1 Single line diagram of the power system network during a fault condition

Table 1 List of symbols used in Fig. 1

Parameter	Description			
	<u>'</u>			
\tilde{I}_M and \tilde{I}_N	Measured phasor currents at bus M and N			
\tilde{E}_M and \tilde{E}_N	Equivalent source voltages at bus M and N			
Z_I	Total positive-sequence line impedance (Ω)			
Z_{m} and Z_{n}	Equivalent source impedances (Ω) at bus M and N			
R_{F}	Fault resistance (Ω)			
δ	Power angle between $\tilde{\it E}_{\it M}$ and $\tilde{\it E}_{\it N}$			
d	Fault distance from bus M to fault point (pu)			
\tilde{l}_{Sum}	Phasor summation of the two-end currents measured at bus M and N.			
F ₁ and F ₂	Represents internal and external faults of protecting zone (line M-N).			
GPS	Global Positioning System			
R	Relay			
СВ	Circuit Breaker			

3 Setting of the restraining region (RR)

The setting of a Restraining Region (RR) plays a fundamental role in the reliability of any protection scheme. To determine the RR, the following mathematical analysis is carried out by considering symmetrical and asymmetrical faults.

3.1 Three-phase internal fault

For a three-phase fault at F_1 as shown in Fig. 1, the fault current at bus M can be expressed in terms of the total fault current at the fault path as:

$$\tilde{I}_{MF} = \left[\frac{(1-d)*Z_l + Z_n}{Z_m + Z_l + Z_n} \right] * \tilde{I}_{Sum}$$
(2)

$$\frac{\tilde{I}_{Sum}}{\tilde{I}_{MF}} = \left[\frac{Z_m + Z_l + Z_n}{(1 - d) * Z_l + Z_n} \right] \tag{3}$$

3.2 Single-phase-to-ground internal fault

For single-phase-to-ground fault at (F_1) as shown in Fig. 1, the relationship between the total fault current and the sequence currents at local bus M is shown in Fig. 2 and expressed as:

$$\tilde{I}_{1Sum} = \left[\frac{Z_{1m} + Z_{l1} + Z_{1n}}{(1 - d) * Z_{l1} + Z_{1n}} \right] * \tilde{I}_{M1F}$$
(4)

$$\tilde{I}_{2Sum} = \left[\frac{Z_{2m} + Z_{l2} + Z_{2n}}{(1 - d) * Z_{l2} + Z_{2n}} \right] * \tilde{I}_{M2F}$$
(5)

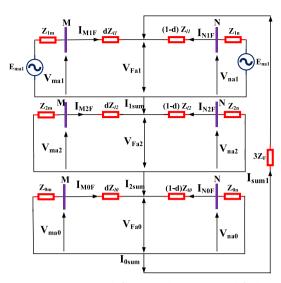


Fig. 2 Sequence network for single line-to-ground fault

$$\tilde{I}_{0Sum} = \left[\frac{Z_{0m} + Z_{l0} + Z_{0n}}{(1 - d) * Z_{l0} + Z_{0n}} \right] * \tilde{I}_{M0F}$$
(6)

For a single-phase-to-ground fault, $Z_{l1} = Z_{l2}$ and $\tilde{I}_{1Sum} = \tilde{I}_{2Sum} = \tilde{I}_{0Sum}$. By adding (4)–(6) and simplifying the zero sequence components, the phase currents can be computed as:

$$\tilde{I}_{Sum} = 2* \left[\frac{Z_{1m} + Z_{l1} + Z_{1n}}{(1 - d)*Z_{l1} + Z_{1n}} \right] * \tilde{I}_{M1F}
+ \left[\frac{Z_{0m} + Z_{l0} + Z_{0n}}{(1 - d)*Z_{l0} + Z_{0n}} \right] * \tilde{I}_{M0F}$$
(7)

$$\tilde{I}_{Sum} = 3* \left[\frac{Z_{1m} + Z_{l1} + Z_{1n}}{(1-d)*Z_{l1} + Z_{1n}} \right] * \tilde{I}_{M1F} + \left\{ \left[\frac{Z_{0m} + Z_{l0} + Z_{0n}}{(1-d)*Z_{l0} + Z_{0n}} \right] - \left[\frac{Z_{1m} + Z_{l1} + Z_{1n}}{(1-d)*Z_{l1} + Z_{1n}} \right] \right\} * \tilde{I}_{M0F}$$

$$(8)$$

$$\frac{\tilde{I}_{Sum}}{\tilde{I}_{MF}} = \left[\frac{Z_{1m} + Z_{l1} + Z_{1n}}{(1 - d) * Z_{l1} + Z_{1n}} \right]
+ \left\{ \left[\frac{Z_{0m} + Z_{l0} + Z_{0n}}{(1 - d) * Z_{l0} + Z_{0n}} \right]
\times - \left[\frac{Z_{1m} + Z_{l1} + Z_{1n}}{(1 - d) * Z_{l1} + Z_{1n}} \right] \right\} * \frac{\tilde{I}_{M0F}}{\tilde{I}_{MF}}$$
(9)

From (3) and (9), it can be seen that the CCR is dependent on the impedances of the source, transmission line, and also on fault location (d). Hence, this analysis is used to set the RR of the proposed scheme.

To determine the RR setting, extensive studies and tests are performed with various operating conditions, considering a 110 kV, 50 Hz transmission system for numerical validation. Here, using (1), the CCR is computed under a normal load condition. To verify the dependability of the scheme, eq. (3) is

used and the CCR is tested with variations of source impedance by simulating an internal 3-phase low resistance fault. To check the security of the scheme, a three-phase fault is created at the external part of the protective zone so the CT will saturate. Furthermore, to validate the sensitivity of the proposed scheme, the CCR is examined using (9) by simulating a high resistance single-phase-to-ground fault, during which the CCR is tested by varying d=0.05 to 0.95 pu. especially for faults at close proximity of the buses. In addition, to check the selectivity of the scheme, it is tested with an external symmetrical fault in the protective zone.

Finally, the following points are noted under these conditions:

- i. During the normal operating condition, the phase angle between the two-end currents is 180^{0} and \tilde{I}_{Sum} is almost zero. However, in practice, \tilde{I}_{Sum} will not be zero because of LCCC and hence the CCR during normal operation is found at 'O' as shown in Fig. 3.
- ii. For a three-phase external fault with low fault resistance (Beyond Bus-N in Fig. 1), the *CCR* is found around 'O'. However, as the fault resistance increases, it is shifted to point 'Z' in Fig. 3.
- iii. For a small load angle, the locus of *CCR* remains at point 'Y'.
- iv. During extreme CT saturation, the *CCR* locus lies at point 'W' in Fig. 3.
- v. For a low resistance external single-phase-to-ground fault, the *CCR* is at 'X' in Fig. 3.

To set the RR, it is necessary to maintain the balance between dependability and security of the relay by controlling the sensitivity. Dependability of a relay can be enhanced by increasing the sensitivity, which is only possible by reducing the area of the RR. However, it is equally important to increase the area of the RR in order to prevent relay mal-operation during

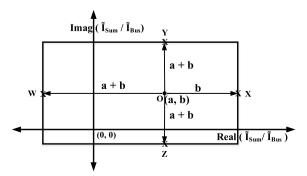


Fig. 3 RR of the proposed scheme

transients and external faults. A high sensitive setting may increase the possibility of relay mal-operation and hence compromises security. It is also possible that errors and inaccuracy in data measurements such as in the instrument transformers can be 1% in magnitude and $0.01\,\mathrm{rad}$ in angle [23]. Measurement uncertainties considered include Gaussian noise of mean zero with a standard deviation of 0.04% in magnitude and 0.017° in angle, and MU (Measurement Units) with the accuracy of $\pm 0.03\%$ in phasor magnitude and $\pm 0.01^\circ$ in phase angle [24].

By considering all the relevant aspects, the following step by step procedures are proposed to construct the RR:

- i. Compute the *CCR* as $\frac{I_{Sum}}{\tilde{I}_{fb}} = a + j b$ under normal operating conditions with maximum normal load angle δ ;
- ii. Locate the *CCR* in a complex current plane as shown in Fig. 3 at 'O';
- iii. Locate point X around a + j b with distance of X along the positive real axis;
- iv. Similarly, locate points X and Y at a distance of (a + b) along the positive and negative imaginary axes, respectively;
- v. Locate another point W by subtracting 'a + b' from 'a + j b';
- vi. Connect all the located points to form a rectangular region as depicted in Fig. 3.

Whenever the locus of CCR travels out of the RR and enters the operating region during a disturbance, the proposed scheme generates the tripping signal.

4 Simulation results and discussion

The 110 kV, 50 Hz, WSCC 9-bus system as shown in Fig. 4 [25] is considered to validate the effectiveness of the proposed scheme. In this system, the line between bus-2 and 3 is chosen as a protective zone to test the

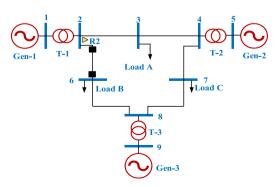


Fig. 4 WSCC 9-bus system for the validation of the proposed scheme

scheme. EMTDC/PSCAD and MATLAB are used for simulation.

To enhance the accuracy of the simulation, the frequency dependent (Bergeron type) transmission line model is considered. The sampling frequency of 1 kHz and window length of 20 ms are used, and current signals are collected using CT (Lucas model-1000/5 A) [26].

A Discrete Fourier Transform (DFT) is used to extract the fundamental components from the measured signals. In the study, the fault is initiated at $0.30\,\mathrm{s}$ and cleared at $0.50\,\mathrm{s}$.

As described in Section III, the setting procedure of RR of the 9-bus system is as follows:

- i. The $\frac{\tilde{I}_{Sum}}{\tilde{J}_{mm}} = a + j b$ value at full load condition with maximum normal load angle of 30° is 0.223 + j 0.08;
- ii. This ratio locates 'O' (0.223, 0.08) in the current complex plane as shown in Fig. 3.
- iii. Point 'X' is marked as (0.303, 0.08) with the distance of b = 0.08 from the point 'O' on the positive real axis.
- iv. Similarly, points Y (0.223, 0.383) and 'Z' (0.223, 0.223) are located on the positive and negative axes of the imaginary line from the reference point 'O'.
- v. The fourth point W (-0.08, 0.08) is located on the negative real axis direction.
- vi. Finally, all 4 points are joined to form a rectangular shape as shown in Fig. 5.

4.1 Variations of loading

In normal operating conditions, the CCR in Line 2–3 mentioned in Fig. 4 is 0.223 + j 0.08 and the corresponding locus is plotted in Fig. 5. Furthermore, it is verified that with 120% and 150% of actual loadings at bus-3, the locus of CCR at both conditions has almost the same ratio at 0.223 + j 0.08 which confirms the effective security of the proposed scheme under loading.

4.2 Internal fault

To examine the dependability of the proposed scheme from internal faults, a three-phase-to-ground fault with fault resistance of $10\,\Omega$ is simulated at the middle of Line 2–3. The corresponding *CCR* can be observed in

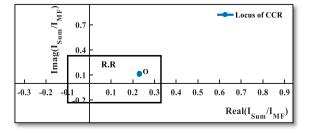


Fig. 5 CCR during normal loading condition

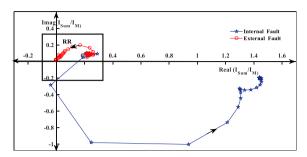


Fig. 6 The CCR for internal and external faults

Fig. 6, where the path of the CCR locus moves far away from the RR and settles almost at (1.42, -0.2) in the operating region.

4.3 External fault

To verify the authenticity of the proposed scheme with external faults, a three-phase-to-ground (ABC-G) fault with $R_{\rm F}$ = 1 Ω is simulated beyond bus-3. The corresponding results are plotted in Fig. 6 where the locus of CCR settles at (–0.01, 0.02) and is within the RR. This demonstrates the security of the proposed scheme under external fault. Hence, Fig. 6 depicts the effective dependability and security of the proposed method.

5 Validation under various operating conditions 5.1 Effect of fault location

To assess the impact of fault location on the proposed scheme, a phase-to-ground (A-G) fault with R_F = 100 Ω , a double-phase-to-ground (AB-G) fault with R_F = 50 Ω and an ABC-G fault with R_F = 10 Ω are simulated along the transmission line, i.e., 0–1 pu. with a step of 0.1 pu. The final points of the *CCR* locus are listed in Table 2. As seen, all the points are

Table 2 Effect of fault location

d (pu)	A-G	AB-G		ABC-G		
	Α	A	В	Α		
0	0.57-0.050j	0.47-0.85j	0.51 + 0.050j	0.63-0.70j		
0.1	0.60-0.051j	0.51-0.84j	0.52+ 0.046j	0.66-0.82j		
0.2	0.62-0.75j	0.53-0.85j	0.57 + 0.041j	0.69-0.75j		
0.3	0.65-0.76j	0.57-0.80j	0.59+ 0.036j	0.71-0.78j		
0.4	0.64-0.78j	0.58-0.78j	0.59 + 0.031j	0.73-0.83j		
0.5	0.66-0.79j	0.60-0.80j	0.61+ 0.025j	0.75-0.56j		
0.6	0.63-0.81j	0.56-0.68j	0.60+ 0.019j	0.76-0.62j		
0.7	0.61-0.82j	0.54-0.69j	0.59 + 0.013j	0.74-0.66j		
8.0	0.57-0.8j	0.51-0.72j	0.55+ 0.006j	0.71-0.67j		
0.9	0.54-0.85j	0.49-0.70j	0.52 + 0.000j	0.69-0.59j		
1.0	0.53-0.86j	0.48-0.58j	0.49 + 0.000j	0.66-0.86j		

settled outside the RR. This guarantees the efficacy of the proposed scheme with respect to fault location.

5.2 Effect of fault resistance

Phase-to-ground faults are most frequent in overhead transmission lines. Conventional transmission line protection schemes such as distance and current differential protection is influenced by fault resistance [1]. To validate the sensitivity of the proposed scheme during high fault resistance, an A-G fault close to bus-3 is simulated with a fault resistance of 200 Ω [27]. The results are depicted in Fig. 7. As seen, the *CCR* starts at point 'O' and moves to the operating region (0.98, -0.2).

Similar results can also be observed at bus-2 at 0.5 pu. length of the line. The corresponding *CCR* can be observed in Fig. 7, in which the locus of the *CCR* settles outside the RR. Thus, it can be acknowledged that the sensitivity of the relay has been verified by the proposed scheme considering high resistance ground faults.

5.3 Test case for CT saturation

The effect of CT saturation plays a very crucial role in differential type protection schemes under external close-in faults. During such conditions, the secondary current of the saturated CT is reduced compared to the actual value. This can cause mal-operation of the relay.

To evaluate the performance of the proposed scheme under CT saturation, an external ABC-G fault is simulated beyond bus-3 with $R_{\rm F}$ = 1 Ω . The CT at bus-2 is designed with the magnetization characteristics as mentioned in [18] to test the saturation effect whereas the CT at bus-3 remains in normal condition. During such a condition, the currents at bus 2 and 3 are measured, as plotted in Fig. 8. CT saturation at bus-2 can be noticed and the corresponding *CCR* locus as plotted in Fig. 9 is restricted to the restraining region which reveals that the system is not affected by CT saturation with the proposed scheme.

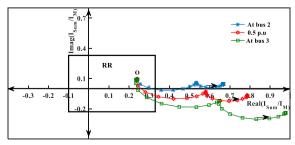


Fig. 7 CCR for single line to a ground fault with $R_F = 200 \Omega$

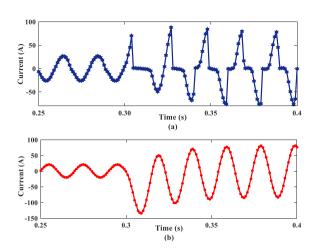


Fig. 8 Fault currents (Phase-A) at (a) Bus-2 (b) Bus-3

5.4 Variation in source impedance

To test the proposed scheme with variations in source impedance, the impedance of generator-1 is varied to be 50%, 100%, 200% and 500% of the actual value [28] while the impedance of generator-2 is kept constant. With these variations, the simulation results are listed in Table 3 considering a three-phase fault. From Table 3, it is seen that the *CCR* during all variations remains in the operating region. This confirms the reliable operation of the proposed scheme.

5.5 Performance on series compensated lines

The nonlinear behavior of a MOV (Metal Oxide Varistor) connected across the series compensated capacitors to protect them from overvoltage creates asymmetry in phase impedance [29]. This operation also depends on pre-fault current, type of fault, fault location, and fault resistance which can cause conventional differential methods to mal-operate. To test the reliable performance of the proposed method, a 50% series compensation is considered at the middle of Line 2–3. An A-G fault with $R_{\rm F}=200\,\Omega$ is simulated and the corresponding results are depicted in Fig. 10. It can be seen that the

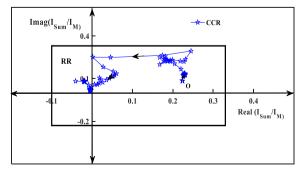


Fig. 9 Effect of CT saturation on the proposed scheme

Table 3 Effect of variations in source impedance

ʻd' (pu)	Percentage of source impedance at Gen-1					
	50%	100%	200%	500%		
0.1	0.48-0.71j	0.55-0.78j	0.53-0.92j	0.58-0.27j		
0.2	0.50-0.80j	0.58-0.72j	0.55-0.77j	0.60-0.32j		
0.3	0.53-0.75j	0.60-0.55j	0.57-0.56j	0.62-0.27j		
0.4	0.58-0.55j	0.63-0.50j	0.60-0.45j	0.65-0.93j		
0.5	0.61-0.52j	0.65-0.65j	0.62 - 033j	0.68-0.86j		
0.6	0.59-0.62j	0.62-0.57j	0.61-0.42j	0.66-0.32j		
0.7	0.56-0.53j	0.58-0.92j	0.58-0.67j	0.64-0.78j		
0.8	0.55-0.92j	0.57-0.86j	0.56-0.82j	0.59-0.62j		
0.9	0.52-0.96j	0.55-0.77j	0.54-0.86j	0.56-0.56j		
1.0	0.47-0.87j	0.49-0.89j	0.53-0.72j	0.55-0.65j		

locus of *CCR* at both cases moves from the restraining region to the operating region. Furthermore, the system with 20%, 30%, and 40% compensation levels are verified and similar results are obtained.

5.6 Effect of power swing

When a power system recovers from disturbances such as fault and/or heavy load rejection, it may experience power swings and the system frequency may diverge from the nominal 50 or 60 Hz condition [30]. Therefore, although there is no fault the system appears to encounter a three-phase fault. To test such an adverse effect, a three-phase fault is simulated at the middle of the line between bus 2–6 as shown in Fig. 4 at 0.8 s and cleared at 1.1 s by opening the respective breakers of the line. Then, by introducing intentional time delay during fault clearance, a power swing is induced in the line between bus 2–3. Figure 11a shows the power swing at bus-2 in which the swing in the phase current starts from 1.1 s and ends at 1.5 s.

During this period (1.1–1.5 s) the *CCR* is computed and plotted in Fig. 11b. As can be seen, the locus of *CCR* in all phases is located inside the RR. This reveals that the proposed scheme has high security from power swing in the power system.

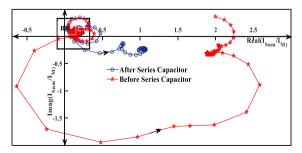


Fig. 10 CCR during faults in series compensated lines (before and after)

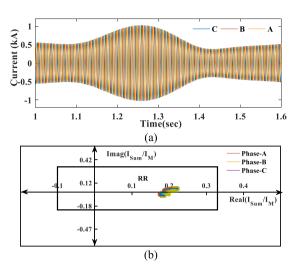


Fig. 11 a CT primary Phase current (kA) during power swing (b) *CCR* during power swing

5.7 Three-phase fault during power swing

Power swing is not directly responsible for power system blackout. However, unintentional tripping during a power swing may cause blackouts or brownouts. On the other hand, if somehow a fault occurs during the swing, the relay should detect the fault and operate quickly.

To test the performance of the proposed scheme during such a power swing condition as shown in Fig. 11a, a three-phase fault is created with $R_{\rm F}$ = 1 Ω at the middle of the protected line (Line 2–3). The fault duration is at 1.3–1.5 s and Fig. 12a shows the current (Phase-A) in

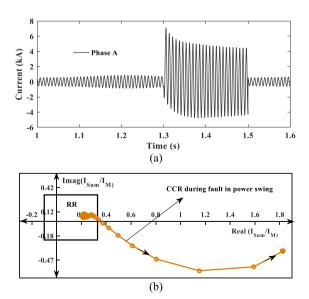


Fig. 12 a CT primary phase current (kA) (**b**) *CCR* during three-phase fault in power swing condition

the line between bus-2 and 3. Figure 12b shows the computed CCR during the three-phase fault at the power swing condition. As can be seen, the CCR moves from the RR to the operating region, and settles at (1.87, -0.32). This confirms the ability of the proposed technique to discriminate the internal fault during a power swing.

6 Comparative assessment

Compared with other schemes specified in the introduction, the effectiveness and advantages of the proposed scheme can be highlighted as follows:

- i. Its performance is not affected by fault resistance whereas traditional current differential protection suffers from this problem [1].
- ii. It provides reliable security from the influence of CT saturation [12–15].
- iii. It eliminates the need for high-speed processors as in the TW-based methods because of the low sampling rate required, e.g., at 1 kHz [16, 17].
- iv. The scheme is not affected by fault type, fault location, fault resistance, and series compensation [30].
- v. Complete protection of the transmission line can be achieved by phase characteristics requiring no negative and zero sequence characteristics [22].
- vi. It is not affected by Single-Pole Tripping (SPT) because of the use of phase elements.

7 Conclusion

In this work, the ratio of phasor summation of the two-end currents to the local end current is defined, instead of the summation of the two-end currents, for fault discrimination. The simulation results show that the proposed scheme is highly reliable for internal faults, having good sensitivity for high resistance faults and security from CT saturation during close-in external faults. Furthermore, the technique is not affected by the fault location, load current, line charging capacitive current and series compensated lines. The performance is also verified under stressed conditions such as a fault during a power swing. In addition, the setting of the operating region is simple and requires no negative and zero sequence characteristics.

Abbreviations

CCR: Complex Current Ratio; CT: Current Transformer; TW: Travelling Wave; DFT: Discrete Fourier Transform; EHV: Extra High Voltage; ETPTL: Equal Transfer Process of Transmission Line; LCCC: Line Charging Capacitive Current; MU: Measurement Unit; SPT: Single Pole Tripping; UHV: Ultra High Voltage; WSCC: Western System Coordinating Council; RR: Restraining Region; MOV: Metal Oxide Varistor

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Authors' contributions

The corresponding author contributed significantly to define problem statement, formulation of new scheme and implementation in simulation tools. The co-corresponding author, contributed his acknowledge during paper writing and improve the quality of the the paper. All the authors read and approved the submitted manuscript.

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