### **ORIGINAL RESEARCH**

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# IEC61850 standard-based harmonic blocking scheme for power transformers



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### **Abstract**

Transformer Differential and overcurrent schemes are traditionally used as main and backup protection respectively. The differential protection relay (SEL487E) has dedicated harmonic restraint function which blocks the relay tripping during the transformer magnetizing inrush conditions. However, the backup overcurrent relay (SEL751A) applied to the transformer protection does not have harmonic restraint element and trip the overcurrent relay during the inrush conditions. Therefore, major contribution of this research work is the developed harmonic blocking scheme for transformer which uses element (87HB) of the transformer differential relay (SEL487E) to send an IEC61850 GOOSE-based harmonic blocking signal to the backup overcurrent relay (SEL751A) to inhibit from tripping during the transformer magnetizing inrush current conditions. The simulation results proved that IEC61850 standard-based protection scheme is faster than the hardwired signals. Therefore, the speed and reliability of the transformer scheme are improved using the IEC61850 standard-based GOOSE applications.

**Keywords:** Transformer protection, Overcurrent protection, Digital protection scheme, Current differential protection, Transformer magnetizing inrush current, Harmonic blocking, IEC 61850, GOOSE message

### 1 Introduction

Transformer failures can be very expensive such as the cost of repairing the transformer, the cost of energy not delivered because of transformer unavailability, and the possible additional cost on spreading damage to adjacent equipment or of a significant power system blackout.

Transformers failures are also dangerous. Internal and external faults and other abnormal operating conditions, such as overload, overexcitation, overvoltage and mechanical stress due to loading on transformers. The transformer protection schemes should disconnect the protected device before extensive damage occurs and/or power system. In addition to protection elements, transformer protection relays should also provide thermal and through-fault monitoring functions. The electrical protection of a transformer includes differential protection, negative sequence percentage differential protection, combined differential and restricted earth protection and the backup overcurrent protection schemes and the mechanical protection of

In 1941, author [1] proposed a new type of relays using the principle of harmonic restraint, which can distinguish between the magnetizing-inrush current and the internal fault current by their difference in the waveform shape. Authors [2] proposed a new digital algorithm to detect winding faults in single-phase and three-phase transformers. This algorithm is suitable to measure winding currents. Various operating conditions were simulated to test the algorithm. In 1997, [3] presented a new method to discriminate internal fault current from inrush current. To avoid unnecessary trip caused by the magnetizing inrush current, the second harmonic component is used to block the differential relays on the power transformers.

IEC 61850 standard has developed two types of models based on peer-to-peer communication, which are Sampled Values (SV) and Generic Object-Oriented Substation Event (GOOSE). IEC 61850 has magnificent features such as high priority, great flexible and reliable mechanism for the fast transmission events of the substation (trips commands, alarms or indications) [4]. Authors [5] used the Phase-Locked Loops (PLL) technology to propose a novel current differential protection scheme. The scheme solves the

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a transformer includes Buchholz relay, pressure protection and thermal protection.

problem of delay-non-determinism, and it also establishes a research platform to show the delay-non-determinism problem using the OPNET Modeller. The proposed method analyses the transferring time delay of sampled values from Non-Conventional Instrument Transformer (NCIT) to the differential protection IED using the IEC 61850 standard network. In this research work, Phase-Locked Loops (PLL) technology is used to implement the time synchronisation between Merging Unit (MU) and IEDs.

In 2009, authors [6] presented a new protection scheme based on IEC 61850–7-2 GOOSE communication. The proposed scheme uses analogue measurements (current and voltage) and digital signals between differential (87) and distance (21) protection functions. As soon as a location of the faulted equipment is identified, it is isolated by the proposed new protection scheme in a coordinated manner entirely by sending a trip signal to both local and remote breakers. Using the IEC 61850 standard technology, every single IED of the proposed scheme also detects the faulted adjacent line, and it sends a trip signal remotely to the corresponding breaker.

The impact of network traffic and sampling synchronisation error on the performance of the transformer differential protection based on IEC 61850 standard was investigated and compared to conventional hardwired connections by authors [7]. To test the transformer differential protection performance caused by synchronisation error between Merging Units (MU), a testbed of precision time protocol (PTP) clocks, protection IED, merging units, and Ethernet switches to be investigated is developed. IEC 61850 GOOSE communication is used to trip Circuit Breakers (CB), report the tap changer position and transduce differential current measurements.

Authors [8], provides five different methods, namely, (1) Harmonic Restraint (HR), (2) conventional Waveform Identification (WI), (3) Fuzzy logic, (4) Wavelet analysis, and (5) Artificial Neural Network (ANN) to discriminate between magnetizing inrush and internal fault conditions. Harmonic Restraint is a typical way of restraining a trip. It is assumed that magnetizing-inrush contains a high level of second harmonic currents which is the HR principle of operation. The HR method uses the magnitude of the second harmonic in the differential current and compares it to the magnitude of the fundamental frequency component. The tripping of the differential element is blocked as soon as the ratio exceeds the set threshold.

The HR method [2] is based on the fact that the second harmonic (sometimes fifth) component of the magnetizing inrush current is considerably larger than a typical fault current. In traditional substations, overcurrent relays are used as a backup protection with time delay higher than that for the main protection. However the main drawback

to realize on backup protection is due to time delay and loss of selectivity which may cause serious impact on the power system.

In smart substation, Intelligent Electronic Devices (IEDs) compliance with IEC61850 standard are deployed to obtain sampling data and state information of other IEDs through IEC61850 communication network which lead to improve the protection performance of the backup protection.

In this research work, transformer current differential protection using SEL487E and its backup overcurrent protection using SEL751A, both IED's support IEC61850–7-4 logical nodes to share their data and communicate their Trip/block signals to the other IEDs on the network. This improves the protection speed and reliability of the backup overcurrent protection scheme using IEC61850 GOOSE communication in comparison with traditional hardwired signals with longer time delay setting. Therefore the research work reported in [9] implemented IEC61850 standard-based differential protection scheme which sent harmonic blocking signal to backup overcurrent relay during inrush current conditions to improve the speed and reliability of the backup protection.

Even-numbered harmonics (second or fourth) provide security during energization, while fifth-harmonic blocking provides security for overexcitation conditions. The research work presented in this manuscript consider second harmonic blocking method to provide security during energization (inrush current conditions) of both main differential and backup overcurrent protection for transformers. Overexcitation conditions are not part of this research work, therefore higher harmonic order such as fifth harmonics onwards not considered in this research work.

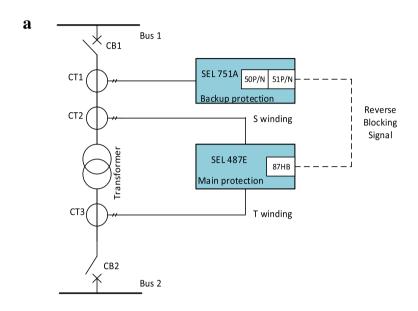
The authors [10] proposed a flux-restrained differential current for power transformer protection. In 1990, [11] presented an algorithm, based on HR, using discrete hartley transform. Different advanced digital filtering algorithms such as Kalman filtering [12], Fourier-based method [13], etc., are used in HR differential protection schemes. However, the HR-based method sometimes fails to prevent false tripping due to high second harmonic components during internal faults. Low second-harmonic components which are generated during magnetizing inrush of the transformers having modern core material. Therefore, the techniques based on detection of the second/fifth harmonic component may not be a proper method to discriminate between the inrush and fault condition on power transformers.

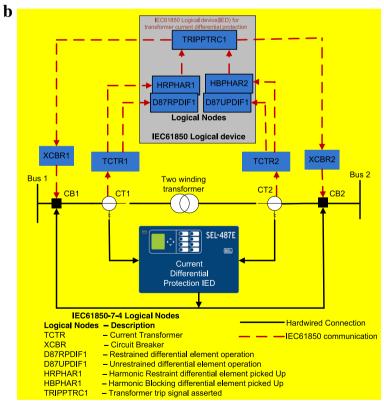
Differential protection and backup overcurrent protection are the most proficient internal faults protection for the power transformer. The differential protection uses differential currents, which result from the difference between HV side and LV side currents and overcurrent uses only primary current. Energization of transformers causes inrush current passing through the transformer coils [14].

The inrush current is a harmonic rich current including slowly decaying DC component [14] because of transformer core saturation which leads to overcurrent relay mal-operation.

The differential transformer protection uses a conventional technique based on the second harmonic

restraint; however, overcurrent relay does not have in-built computation for harmonic function in order to discriminate between an internal fault and inrush currents. This leads to the trip of the elements of the backup overcurrent relay due to transformer magnetizing inrush current conditions which affect the





**Fig. 1 a** Harmonic Blocking scheme for power transformer protection. **b** Physical and IEC61850 -based virtual connection for current differential protection scheme

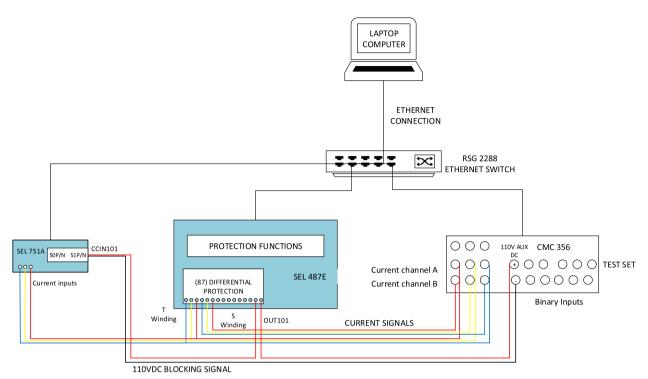


Fig. 2 Implementation of the Harmonic Blocking scheme

power systems stability. Therefore, the research project was motivated to develop a new method to prevent the malfunction of the backup overcurrent relay due to the transformer magnetizing-inrush current conditions.

The digital protection algorithms that were proposed in the past for protecting power transformers have been focused on using transformer differential protection. Most of the research work reviewed is concentrating on solving the differentiation between inrush current and internal faults on the main transformer protection relay and failed to focus on backup overcurrent. Therefore, this research work is focused on IEC 61850 standard-based harmonic blocking method to prevent the backup overcurrent relay from tripping during inrush current conditions. This paper provides the test bench implementation for the harmonic blocking scheme using both hardwired DC signal and IEC 61850 standard-based GOOSE message. The developed algorithm for the harmonic blocking scheme is presented. Two case studies are studied, one for the malfunction of the SEL-751A IED due to TMIC and another one to prevent the tripping of the SEL-751A IED due to TMIC using the harmonic blocking scheme.



Fig. 3 Test bench setup for transformer Harmonic Blocking scheme using current differential function

## 2 IEC61850 standardization to transformer harmonic blocking function

IEC61850 Ethernet-based communication provides interoperability between intelligent devices within the substation and allow standardized and interconnection of intelligent devices from different manufacturers for protection, monitoring, control of the substation. Transformer differential relay (SEL487E) has both harmonic blocking and harmonic restraint functions to obtain relay stability during transformer inrush current conditions. According to standard IEC61850-7-4 there are dedicated logical node classes and its corresponding data classes for every single protection, metering and control functions. Figure 1a provides both physical hardwired connection and virtual IEC61850 GOOSE messagebased communication for transformer differential protection scheme.

The bottom section of the Fig. 1a provides physical hardwired connection (Black colored) and top section of the Fig. 1a provide virtual connection using IEC61850 GOOSE message-based communication (Red colored)

for transformer differential protection scheme. In IEC61850 standard each physical power system components (CTs, relay functions and breakers) are represented with its corresponding logical node classes and its corresponding data attributes. In research work [9], logical node HBPHAR2 or its relay word bit 87HB of harmonic blocking function of differential element is used to send IEC61850-based GOOSE message blocking signal to the backup overcurrent relay during transformer inrush current conditions as shown in Fig. 1a and b respectively to avoid misopereation of the backup overcurrent relay during inrush current conditions. The filtered differential relay element blocks all phases when the harmonic magnitude of any phases exceeds the harmonic setting.

### 3 Test bench set-up of the harmonic blocking scheme

During transformer energisation or recovery from a system fault, a substantial amount of inrush currents flows into the transformer without a corresponding current leaving. The differential relay has the capability to detect

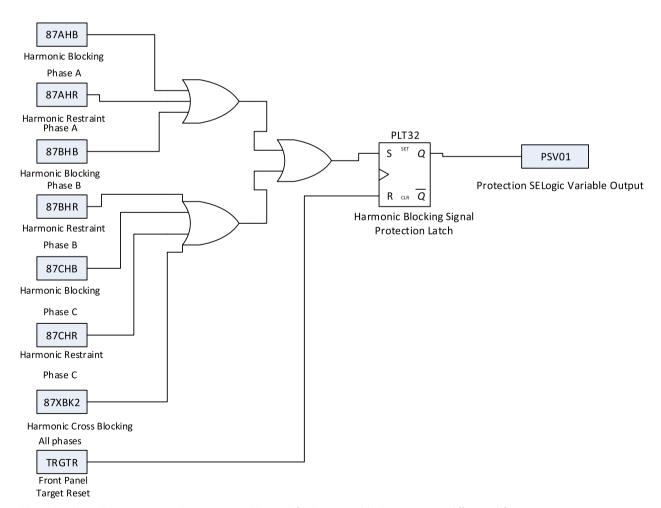


Fig. 4 Developed SELogic control equations in SEL-487E for harmonic blocking/restraint differential function

an inrush condition and restrain itself from tripping. However, the overcurrent relay employed as backup protection does not have inrush current feature.

In order to restrain the SEL 751A overcurrent relay from tripping during inrush conditions, a blocking scheme based on harmonic currents is employed. The scheme uses the Harmonic Blocking element (87HB) of the SEL 487E IED to send a blocking signal to the SEL 751A IED at upstream of the network to inhibit it from tripping during inrush conditions as shown in Fig. 1b.

As soon as currents are fed into the IEDs by the CTs (CT1, CT2 and CT3) as shown in Fig. 1b, the SEL 487E and SEL 751A perform Discrete Fourier Transform (DFT) signal processing and calculate internal protection function to determine which element is asserted and de-asserted. During Transformer Magnetizing Inrush Current (TMIC), if the calculated second harmonic values of the primary currents exceed the pickup or setting value, the Harmonic Blocking element (87HB) of the SEL 487E asserts and restrain the SEL 487E from tripping. While asserted, the 87HB element transmits a blocking signal to the SEL 751A to restrain from tripping due to TMIC condition as shown in Fig. 1b. To verify and investigate the performance of the harmonic blocking scheme, a test bench is developed and is shown in Figs. 2 and 3 respectively.

The test bench consists of the following equipment: SEL 487E IED, SEL 751A IED, Omicron CMC 356 Test set, RUGGEDCOM RSG 2288 Ethernet switch and the

personal computer with AcSELerator Quickset application to perform engineering configuration for the numerical relay and AcSELerator Architect IEC 61850 engineering configuration software tool.

In Fig. 2, the OMICRON test set is used to inject the inrush currents from channel A and B of the CMC 356 into the protection IEDs (SEL-487E and SEL-751A). The S winding of the SEL 487E is connected in series with the SEL 751A via current channel A of the CMC test set.

This is because the S winding of SEL-487E and the SEL 751A backup overcurrent relay both measure currents on the primary winding of the power transformer. CMC 356 device is used to provide 110 DC voltage which is used to interlock the two IEDs (SEL-487E and SEL-751A) as shown in Fig. 2. The T winding secondary side of the power transformer is connected to current channel B of the CMC 356 test set. The IEDs (SEL-487E and SEL-751A), CMC 35 and a laptop with engineering configuration tools are connected in the network using the Ethernet protocol for substation communication.

The harmonic blocking scheme is implemented using both hardwired signals and IEC 61850 standard-based GOOSE message. To achieve the harmonic blocking scheme, the SEL-487E and SEL-751A need to be configured using the given SELogic control Eqs. (1) to (8) to produce a blocking signal whenever the harmonic blocking element picks up an inrush condition on any one of the three phases.

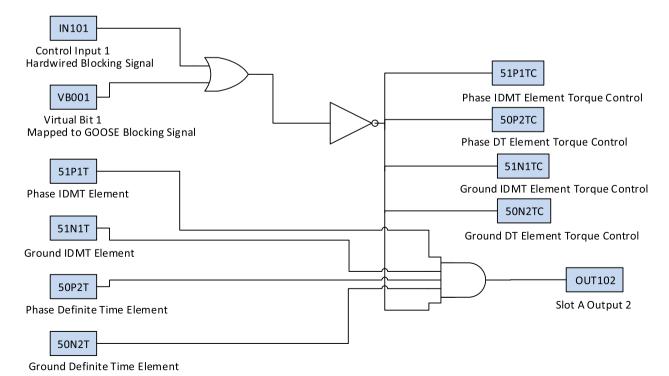


Fig. 5 Developed SELogic control equations in SEL-751A for the implementation of the Harmonic Blocking scheme

To avoid SEL-751A relay mis-operation during inrush conditions the filtered differential element uses harmonics to either block or restrain the differential element. The SEL-487E relay blocks all the phases when the harmonic magnitude of any one of the three phases excesses the harmonic setting. Even numbered harmonics (second and fourth) provide security during transformer energisation, while fifth-harmonic provides security for overexcitation conditions. Harmonic blocking and harmonic restraint provide a good balance between speed and security. The harmonic blocking element includes common (cross) second and fourth harmonic blocking and independent fifth harmonic blocking for improved security.

To verify the performance of the harmonic blocking scheme, the scheme is implemented as depicted in Fig. 4 below.

### 4 Developed SELogic control equations for the harmonic blocking scheme

In order for the SEL 487E to generate a harmonic blocking signal, the following SELogic control Eqs. (1) to (3) were created in AcSELerator Quickset Engineering tool:

$$PLT32S = 87AHB OR 87AHR OR87BHB OR$$

$$87BHR OR87CHB OR87CHR$$

$$(1)$$

$$PLT32R = TRGTR (2)$$

$$PSV01 = PLT32 \tag{3}$$

graphical logic representation of this free-form SELogic control Eqs. (1) to (3) is shown in Fig. 4.

From the Fig. 4, it is discernible that any asserted phase harmonic restraint or blocking elements (87HB or 87HR) will set the protection latch PLT32, which

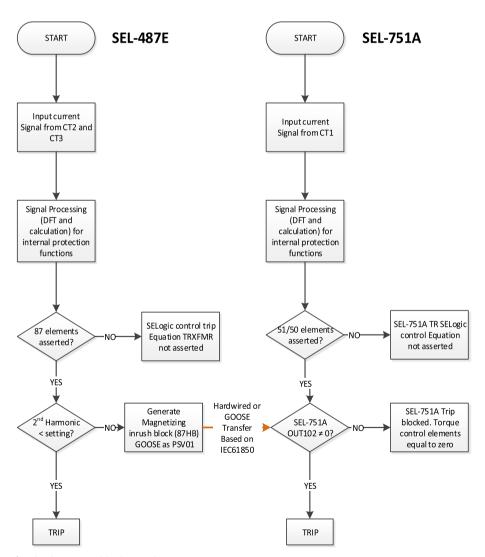


Fig. 6 Flowchart for the harmonic blocking scheme

asserts the protection SELogic variable PSV01 which is mapped to OUT101 output port of SEL-487E. The protection latch PLT32 is used to latch in the harmonic signal because either harmonic blocking or restraint elements (87HB or 87HR) do not assert continuously. The status value of the protection SELogic variable PVS01 is transmitted as the blocking signal as shown in Fig. 4.

In order to restrain the SEL 751A overcurrent IED from tripping during transformer inrush condition upon receipt of the blocking signal from SEL-487E, the following SELogic control equations are created in AcSELerator Quickset:

$$51P1TC = NOT(IN101 OR VB001) \tag{4}$$

$$51N1TC = NOT(IN101 OR VB001)$$
 (5)

$$50P2TC = NOT(IN101 OR VB001)$$
 (6)

$$50N1TC = NOT(IN101ORVB001)$$
 (7)

OUT102 = NOT(IN101 OR VB001) AND (51P1T OR51N1T OR50P2T OR50N1T)

(8)

The torque control elements 51P1TC, 51N1TC, 50P2TC and 50N2TC, are used to interlock the 51P, 51 N, 50P and 50 N elements and avert them from asserting during inrush conditions as shown in Fig. 5. Under normal conditions (no TMIC) the control input IN101 and the virtual bit VB001 carry a logical value of 0. Applying this logical state to a NOT gate

produces a high logical state, which guarantees that the torque-controlled elements 51P, 51 N, 50P, and 50 N can still assert if a fault occurs on the system. Output 102 is also interlocked to the blocking signal to ensure that no other element of the SEL-751A IED can energise this output and pass a trip signal onto the circuit breaker during inrush conditions. The graphical logic representation of free-form SELogic control equations is shown in Fig. 5.

# 5 Algorithm to implement the harmonic blocking scheme using hardwired and IEC 61850 standard-based GOOSE message

SEL-751A IED does not have an inbuilt function for harmonic blocking so whenever the power transformer energises, the TMIC asserts 50 & 51 elements of the backup protection IED SEL-751A as shown in Figs. 2 and 3. To block the 50 & 51 elements from tripping during TMIC condition, harmonic blocking scheme algorithm is implemented using hardwired, and IEC 61850 standard-based GOOSE message and is described in detail in this section.

Steps to implement the harmonic blocking scheme algorithm using IEC 61850 standard-based GOOSE message are as follows:

SEL-487E power transformer IED performs a
 Discrete Fourier Transform (DFT) signal processing
 using input current signals from the current
 transformers CT2 and CT3 connected to S and T
 windings respectively as shown in Fig. 1b.

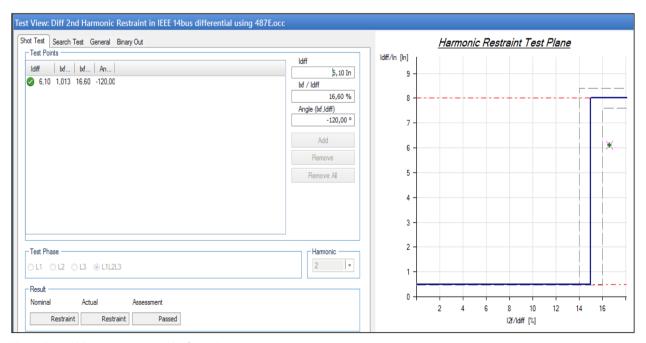
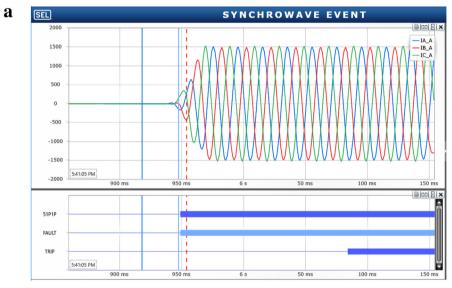


Fig. 7 Second harmonic test results from Omicron test universe

- 2. Calculate the internal protection function on SEL-487E using DFT signals from step 1.
- 3. For internal faults on the power transformer, the corresponding relay word bit 87 T is asserted. SEL-487E performs the second-harmonic ratio calculation in the differential currents, for internal faults obviously the 2nd harmonic will be less than the threshold setting value. Relay sends a trip signal to the circuit breakers CB1 and CB2 across the power transformer as shown in Fig. 1b.
- 4. During TMIC conditions, SEL-487E performs the second-harmonic ratio calculation again. If the 2nd harmonic primary current exceeds its pickup setting, then the harmonic blocking elements

- (87HB and 87HR) are asserted and restrain the relay from tripping.
- 5. After successful completion of step 4, SEL-487E transfers a magnetizing inrush blocking (87HB) signal as protection SELogic variable (PSV01) to SEL-751A IED using hardwired and IEC 61850 standard-based GOOSE message
- 6. SEL-751A overcurrent IED performs a Discrete Fourier Transform (DFT) signal and processing using the input currents from the current transformer CT1 connected at the primary side of the power transformer. SEL-751A is used as a backup protection for the power transformer SEL-487E IED as shown in Fig. 1b



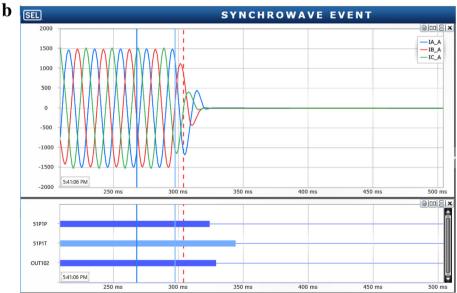


Fig. 8 a SEL-751A current signals during transformer inrush current condition. b SEL-751A trip signal during transformer inrush current condition



Fig. 9 Harmonic blocking signal wiring diagram

- 7. SEL-751A IED checks whether phase definitetime overcurrent (50) or phase time-overcurrent (51) elements are asserted for internal events.
- 8. For internal faults described in step 7 on the protection zone of the power transformer, the corresponding relay word bits  $50\,\mathrm{T}$  or  $51\,\mathrm{T}$  is

- asserted and the circuit breaker CB1 connected at the primary of the power transformer clears the faults as shown in Fig. 1b.
- 9. However, during TMIC condition SEL-751A receives the magnetizing inrush blocking signals transferred by SEL-487E from step 5 in order to de-assert the relay word bits 50 and 51 from tripping.
- 10. The transfer of magnetizing inrush blocking signal is implemented using hardwired DC signals which are mapped to the input (IN101) as shown in Fig. 5 and IEC 61850 standard-based GOOSE message which is mapped to virtual bit

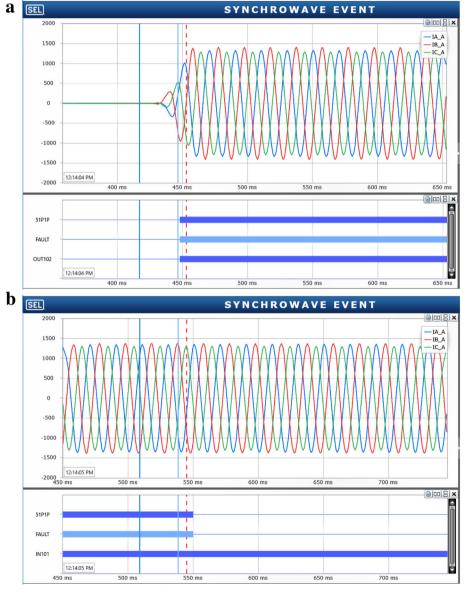


Fig. 10 a SEL-751A recorded signals during inrush current conditions. b SEL-751A overcurrent relay response during transformer inrush current conditions

- (VB001) as shown in Eq. (8) and the diagram shown in Fig. 5. Output 102 is interlocked to the blocking signal to ensure that either 50 or 51 elements of the SEL-751A IED cannot energise the output (OUT102).
- 11. Finally, the protection speed, reliability and performance of the harmonic blocking scheme is analysed using hardwired and IEC 61850 standard-based GOOSE message. A flowchart for the harmonic blocking scheme algorithm is depicted in Fig. 6 below. Two case studies are considered, one with the scheme implemented using traditional hardwiring signals and other with IEC 61850 standard-based GOOSE message replacing the traditional hardwiring signals and the results of each case study are presented and discussed.

### 6 Simulation test results of the harmonic blocking scheme using hardwired signals

The following two case studies are investigated, they are:

- Case study one Investigation of the malfunction of the SEL-751A IED due to Transformer Magnetizing Inrush Current (TMIC)
- Case study two Application of the harmonic blocking scheme to prevent malfunctioning of the SEL-751A due to TMIC

### 6.1 Case study one: investigation of the malfunction of the SEL-751A IED due to TMIC

This case study aims to investigate the performance of the SEL 751A overcurrent relay installed on the upstream of the network during transformer magnetisation inrush current conditions. The SEL-751A IED is tested without the implementation of the developed harmonic blocking scheme. There is a high harmonic content in the inrush currents; however, the fault currents have less harmonic contents that are less than 15%. Therefore, the way to test the inrush current condition is by generating differential currents with harmonic content above 15%. The omicron CMC 356 test set is used to inject currents with a 2nd harmonic level percentage of 16.60% into the SEL-487E and SEL-751A IEDs respectively as shown in Fig. 7.

The pickup differential current is set to 0.5 A and CT ratio set to 400A at the primary side of the power transformer, the test factor selected is 6.10 times the nominal current (6.10 X 400A) = 2440A. Therefore, the Omicron second harmonic simulation currents for L1-L2-L3 to be injected to the IEDs is (2440A X 0.5) = 1220A. The results obtained from the hardwired simulation test are presented in Fig. 8a and b respectively. Figure 8a shows that 16.60% of the 2nd harmonic currents injected in both IEDs (SEL-487E and SEL-751A), in which SEL-751A IED picks up this injected 2nd harmonic current as a fault by asserting inverse time-overcurrent (51P1P) and FAULT elements at 5.95 s.

In Fig. 8b, shows that the inverse definite minimum time element 51P1 of SEL 751A overcurrent relay

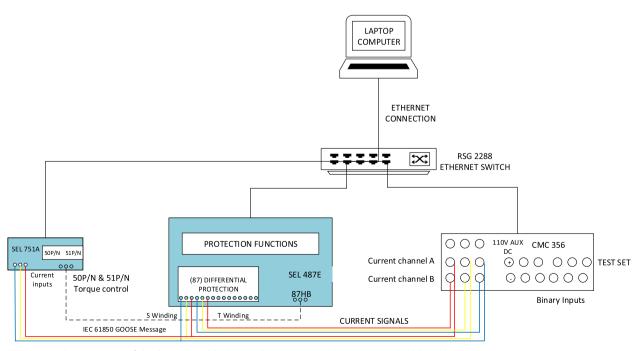


Fig. 11 Implementation of the harmonic blocking scheme using IEC 61850 standard-based GOOSE message

asserted for the 2nd harmonic inrush current which produces a trip signal (51P1T) at  $0.36\,s$  (6.31 s - 5.95 s =  $0.36\,s$ ). It is also evident from the Fig. 8b that no blocking signal sent to SEL-751A IED from SEL-487E in order to restrain the TRIP and 51P1T elements due to TMIC conditions.

# 6.2 Case study two: application of the harmonic blocking scheme to prevent malfunctioning of the SEL-751A due to TMIC using hardwired signals

The aim of this case study is to investigate the harmonic blocking scheme during transformer inrush conditions. This scheme uses a 110 V DC signal looped between SEL 751A and SEL 487E IEDs as

SEL

shown in Fig. 9. The  $110\,\mathrm{V}\,\mathrm{DC}$  signal is wired in series with the normally open output contact OUT101 of the SEL 487E as shown in Fig. 9. The normally open contact, that is output 102 of the SEL 487E is mapped to the protection SELogic variable PSV01 and transition to a closed position and pass the blocking signal to the control input CCIN101 of the SEL 751A when PSV01 asserts.

As shown in Fig. 9, the relay is tested with the developed harmonic blocking scheme. The omicron CMC 356 test set is used to inject differential currents with 16.60% of 2nd harmonic content into the IEDs. The results obtained from the hardwired test simulation is given in Fig. 10a and b respectively.

Figure 10a shows that 16.60% of the 2nd harmonic currents injected in both IEDs SEL-487E and

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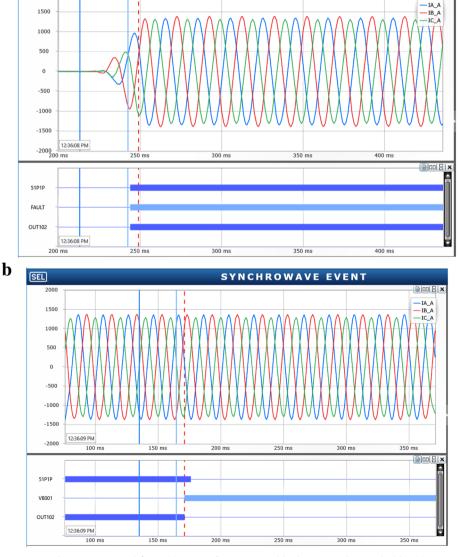


Fig. 12 a Inrush current condition monitored from SEL-751A. b Harmonic blocking signal recorded by SEL-751A

SEL-751A respectively, in which SEL-751A IED picks up this injected 2nd harmonic current as a fault by asserting inverse time-overcurrent (51P1P) and FAULT elements at approximately 4.45 s.

Figure 10b shows that the pickup elements 51P1P and FAULTS are de-asserted at 5.50 s, and the SEL-751A relay does not produce any trip signal. This is because the overcurrent elements are being blocked from asserting by the blocking signal being received through control input IN101. The results of this test also indicate that the malfunctioning caused by transformer magnetisation inrush currents can be prevented by implementing the harmonic blocking scheme.

# 7 Implementation of the harmonic blocking scheme using IEC 61850 standard-based GOOSE message

Harmonic blocking scheme test bench implementation to prevent the operation of the SEL-751A overcurrent elements (51P1 & 50P1) during the transformer magnetizing inrush current conditions is given in Fig. 11.

Omicron CMC356 test set is used to inject the inrush currents into the SEL 487E and SEL 751A IEDs. The S winding of the SEL 487E is connected in series with the SEL 751A current inputs. This is because the S winding and the SEL 751A backup overcurrent relay both measure the current on the primary winding of the protected transformer. The RUGGEDCOM Ethernet switch links the two protective IEDs with the personal computer and the CMC 356 test via a virtual local area network VLAN. The harmonic blocking (87HB) signal is transmitted through Ethernet as a GOOSE message to block the torque control overcurrent elements (50/51 TC) as shown in Fig. 11.

# **7.1** Simulation results analysis of the harmonic blocking scheme using IEC 61850 standard-based GOOSE message The GOOSE simulation results of the developed harmonic blocking scheme are shown in Fig. 12. An inrush current with 16.60% of the harmonic level is injected into the IEDs.

Even-numbered harmonics (second or fourth) provide security during energization, while fifth-harmonic blocking provides security for overexcitation conditions. The research work presented in this manuscript consider second harmonic blocking method to provide security during energization (inrush current conditions) of both main differential and backup overcurrent protection for transformers. Overexcitation conditions are not part of this research work, therefore higher harmonic order such as fifth harmonics onwards not considered. This research work consider second harmonic blocking method to provide security and block the main differential and backup overcurrent relays during transformer inrush current conditions.

The analogue and digital signals recorded during the simulation are shown in Fig. 12a and b respectively. From Fig. 12a, it is observed that with a 16.60% second harmonic currents are injected in both IEDs SEL-487E and SEL-751A respectively. SEL-751A relay this picks up as fault by asserting 51P1P and FAULT elements at 8.250 s.

In Fig. 12b, the digital signals 51P1P represents the phase Inverse Definite Minimum Time (IDMT) element. 51P1P element asserts when the fault on the system and 51P1T should assert when the element issues a trip signal. VB001 is the virtual SELogic protection variable that is mapped to the incoming GOOSE message from SEL-487E received at 9.170 s. It is evident that upon

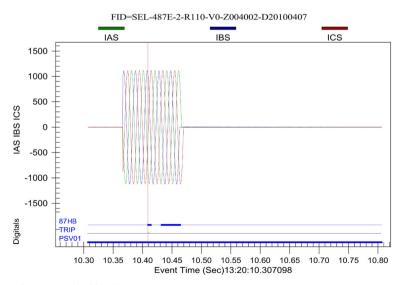


Fig. 13 Inrush current condition recorded by SEL-487E

receipt of the GOOSE message, the 51P1P element dropped out, preventing the relay from issuing a trip signal during TMIC condition. The signals recorded by SEL-487E during the fault are shown in Fig. 13.

In Fig. 13, harmonic blocking element (87HB) digital signal and the protection SELogic variable (PSV01) configured to transmit a harmonic blocking GOOSE message signal during an inrush condition. Although the harmonic blocking element 87HB asserts and de-asserts, the state of the protection SELogic variable PSV01 remains stable. These because the signal is sealed in the SELogic protection latch PLT 32 Eqs. (1) to (3) as soon as the harmonic blocking element asserts for the first time.

The results of the IEC 61850 GOOSE message-based simulation prove that the harmonic blocking scheme can be employed to prevent the tripping of the SEL-751A relay malfunction due to the transformer magnetisation inrush current condition as shown in Fig. 13. Hardwired and GOOSE simulation results are analysed. The simulation results proved that IEC61850 standard-based protection scheme is faster than the hardwired. Table 1 provides the hardwired and GOOSE blocking signals times.

Therefore, the performance of the protection speed and reliability are improved using the IEC61850 standard-based GOOSE applications to the transformer digital protective relaying system and the installation and maintenance expenditure are reduced.

### **8 Conclusion**

The IEC 61850 GOOSE message and hardwired signals-based simulation study was conducted in the lab, and various faults pertaining to power transformers were simulated using the omicron test injection device, and relay performance was monitored. The implementation of the lab-scale test bench setup for transformer protection is presented in Fig. 3.

This paper presents the practical implementation of the IEC 61850 standard based transformer protection scheme. The scheme applies IEC 61850 GOOSE messaging to send a harmonic blocking scheme from the SEL-487E differential IED to the SEL-751A overcurrent IED during the transformer magnetizing inrush current condition.

In addition to that, the developed algorithm for the harmonic blocking scheme is presented in this paper. The test bench setup is implemented for both hardwired DC

**Table 1** Comparison of the current magnitude of the hardwired DC signals and IEC61850 GOOSE blocking signal times

9	3 3	
Type of signal	Hardwired signal	GOOSE Message
Current Magnitude	1220A	1220A
Blocking time	5.55-4.45 = 1.1 s	9.17-8.25 = 0.92 s

signals and IEC 61850 GOOSE message signals for harmonic blocking for transformer differential elements. Two case studies are simulated in order to analyse the performance of the transformer protection speed, security and reliability of the developed harmonic blocking scheme.

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#### Availability of data and materials

Not applicable.

### Authors' contributions

SK supervised this research work and participated in development of the harmonic blocking algorithm for power transformers and helped to draft the manuscript. SK also proof read and approved the final manuscript. SK revised the manuscript and respond to the reviewer comments. BE carried out the test bed setup in the CSAEMS laboratory using SEL487E, SEL751A IEDs and Omicron test injection devices and demonstrated the harmonic blocking scheme for transformer inrush currents and drafted the manuscript.

#### Competing interests

The authors declare that they have no competing interests.

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