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Fault identification scheme for protection and adaptive reclosing in a hybrid multi-terminal HVDC system



Junjie Hou^{1*}, Guobing Song^{1,2} and Yanfang Fan¹

Abstract

A fault identification scheme for protection and adaptive reclosing is proposed for a hybrid multi-terminal HVDC system to increase the reliability of fault isolation and reclosing. By analyzing the "zero passing" characteristic of current at the local end during the converter capacitor discharge stage, the fault identification scheme is proposed. The distributed parameter-based fault location equation, which incorporates fault distance and fault impedance, is developed with the injection signal and the distributed parameter model during the adaptive reclosing stage. The fault distance is determined using a trust region reflection algorithm to identify the permanent fault, and a fault identification scheme for adaptive reclosing is developed. Simulation results show that the proposed scheme is suitable for long-distance transmission lines with strong anti-fault impedance and anti-interference performance. Also, it is less affected by communication delay and DC boundary strength than existing methods.

Keywords Adaptive reclosing, Hybrid multi-terminal HVDC system, Protection, Signal injection

1 Introduction

Traditional high voltage direct current (HVDC) systems using a line-commutated converter (LCC) are often used owing to their large capacity and longer transmission distance advantages. Such HVDC technology progress is nonetheless constrained by commutation failure. Voltage source converters (VSC) using fully controlled power electronic switches have significant potential for development in HVDC systems owing to their higher controllability and avoidance of commutation failure [1]. However, in a practical HVDC project, if VSC is used, its cost usually restricts project development. As a result, the hybrid HVDC system, which integrates traditional LCC

*Correspondence:

826686025@qq.com

Xinjiang 830046, China

and VSC converters, has a wide range of applications. A hybrid HVDC system provides significant transmission capacity and longer transmission distance, eliminates the risk of commutation failure, and decreases the cost [2].

Given the advantages of a multi-terminal power network, hybrid multi-terminal HVDC systems, such as the Wudongde hybrid multi-terminal HVDC transmission system, have a wide range of application prospects as HVDC research progresses [3]. The system uses a T-shape topology comprising an LCC at the sending terminal and two hybrid modular multilevel converters (MMC) at the receiving terminals. The negative level output capability of the hybrid MMC provides fault current self-clearing [4]. Compared with the half-bridge MMC (HB-MMC), the DC boundary strength required by the hybrid MMC will be further weakened [5]. Nevertheless, because of the peculiarity of the T-shape topology, identifying the fault area based on the DC boundary is complicated.

Currently, the protection principles of the hybrid multi-terminal HVDC grid mainly focus on single-ended



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Junjie Hou

¹ The School of Electrical Engineering, Xinjiang University,

² The School of Electrical Engineering, Xi'an Jiaotong University, Shanxi 710049, China

protection [6-9] and pilot protection [3, 10-12]. Generally, the single-end protection principle of the hybrid multi-terminal DC transmission system depends on wavefront identification, and its performance is closely related to the sampling rate, wavefront calibration, DC boundary, fault locations, etc., and requires further development. The pilot protection principle for the hybrid multi-terminal HVDC transmission system mainly depends on current polarity characteristics or traveling wave transmission theory. As a result, the performance is affected by fluctuations in electrical quantities, wavefront calibration, sampling rate, etc. Moreover, in the case of long-distance transmission lines, the pilot protection principle is vulnerable to transmission delay and calculation error at the two ends. Thus its performance needs to be further enhanced.

Currently, injection adaptive reclosure methods [13– 15] are generally based on traveling wave transmission theory. However, the traveling wave transmission process can be influenced by the sampling rate, DC boundary, fault position, accuracy of wavefront identification and other parameters [15–18], and thus its performance requires further improvement. References [19, 20] use the fault analysis method to identify the fault properties of the line, but the performance analysis of the line length and fault impedance requires additional investigation.

Existing research has the following problems:

- Most fault detection schemes rely on the DC boundary, so their effectiveness needs to be investigated further when the DC boundary weakens or vanishes.
- Most existing fault identification schemes use traveling wave transmission theory. Nevertheless, fault impedance, sampling rate, wavefront calibration, special fault location, and other factors can affect the performance of these traditional methods, reducing protection performance.
- Most fault identification schemes are only for protection or reclosing while ignoring fault identification schemes in the whole fault process.

Thus, this paper proposes a fault identification scheme for protection and adaptive reclosing for a hybrid multiterminal HVDC system. The proposed scheme has the following main features:

• In the protection stage, the "zero-passing" characteristics of the current at the local end during the capacitor discharge stage are used to quickly identify the fault area without a long communication delay and complex mathematical calculation.

- In the adaptive reclosing stage, the proposed method can sensitively identify the fault properties and has the fault location function. In addition, it does not need to set the setting values via simulation.
- The proposed scheme is suitable for long transmission lines during the whole fault process and has strong anti-fault impedance and anti-interference performance. In addition, it is less affected by the influence of the DC boundary and sampling rate than existing methods.

The rest of the paper is structured as follows. Section 2 analyzes the current characteristics in the capacitor discharge stage, and the "zero-passing" characteristic of the current at the local end is used to identify the fault area. In Sect. 3, a fault identification scheme for adaptive reclosing is proposed, one which considers the influence of distributed parameters and the fault branch downstream. It can identify as well as locate permanent faults. The proposed fault identification scheme flow chart for protection and adaptive reclosing is given in Sect. 4, while its performance in various fault scenarios is verified in Sect. 5. Conclusions are provided in Sect. 6.

2 Fault identification scheme for protection

The hybrid multi-terminal HVDC system is depicted in Fig. 1. An LCC rectifier is used at the sending terminal, and two hybrid MMCs used as inverters are installed at the receiving terminals. The LCC uses constant current control, whereas the two MMCs employ constant voltage and active power control. The DC fault stage is divided into capacitor discharge and a current limiting stage.

In Fig. 1, *a*, *b*, *c*, *d* are the protection installations of the positive lines, whereas a', b', c', d' are the protection installations of the negative lines. L_{dc} denotes the current limiting reactor.



Fig. 1 The topology of hybrid multi-terminal HVDC system

2.1 Fault current characteristics

For the hybrid multi-terminal HVDC system, the capacitor discharge stage is dominant, during which the DC fault current rises rapidly, given as [25]:

$$\begin{split} i_{\rm dc}(t) &= -\frac{1}{\sin \theta_{\rm dc}'} i_{\rm dc(0)} e^{-\frac{t}{\tau_{\rm dc}}} \sin(\omega_{\rm dc}t - \theta_{\rm dc}) + \frac{u_{\rm dc}}{R_{\rm dis}} e^{-\frac{t}{\tau_{\rm dc}}} \sin(\omega_{\rm dc}t) \\ \tau_{\rm dc} &= \frac{4L_0 + 6L_{\rm dc}}{2R_0 + 3R_{\rm dc}} \\ \omega_{\rm dc} &= \sqrt{\frac{2N(2L_{\rm arm} + 3L_{\rm dc}) - C_0(2R_{\rm arm} + 3L_{\rm dc})^2}{4C_0(2L_{\rm arm} + 3L_{\rm dc})^2}} \\ \theta_{\rm dc} &= \arctan(\tau_{\rm dc}\omega_{\rm dc}) \\ R_{\rm dis} &= \sqrt{\frac{2N(2L_{\rm arm} + 3L_{\rm dc}) - C_0(2R_{\rm arm} + 3L_{\rm dc})^2}{36C_0}} \end{split}$$
(1)

where $R_{\rm dis}$, $L_{\rm arm}$, and $R_{\rm arm}$ represent the equivalent resistance of the MMC side, and the equivalent inductance and resistance of the arm, respectively. C_0 is the submodule capacitance, while $\theta_{\rm dc}$ and $\omega_{\rm dc}$ are the initial phase and angular frequency of the DC current, respectively. $i_{\rm dc(0)}$ and $u_{\rm dc}$ are the DC current and voltage in normal conditions.

In the case of a positive pole-to-ground (PTG) fault, the positive current direction is assigned as the bus flow direction line. Figure 2 shows a single pole example (i.e., the positive pole) where i_1 and i_2 are the capacitor discharge currents from protection installations at locations *b* and *a*, respectively, and i_0 is the load current before the fault.

The fault current i_b and i_a at locations b and a can be expressed as:

$$\begin{cases} i_b = i_0 + i_1 \\ i_a = i_0 + i_2 \end{cases}$$
(2)

Since the directions of the load current and the capacitor discharge current are opposite, the fault current will have a "zero-passing" characteristic while increasing in the opposite direction for the protection installation at terminal b. When combined with (1), protection installation a has the same current characteristics as protection installation b. The capacitor discharge stage mainly dominates the fault currents of the two terminals. The direction of fault current is initially

Fig. 2 The current direction of the capacitor discharge stage

determined by the direction of load current and then by the direction of capacitor discharge.

The fault identification scheme is constructed based on the fault current characteristics (i.e., capacitor-discharge stage and fault current limiting stage). The three fault areas T_1 , T_2 , and T_3 can be used to categorize DC system faults. The faults in the T-shaped area are classified as T_3 area (f_3 faults), while T_1 and T_2 denote the faults (f_1 and f_2 faults) that occur on the left and right sides of T_3 , respectively.

Pole-to-pole (PTP) faults that occur on T_1 are taken as the next example. The direction of fault current flow measured at protection installations *b* and *a* of the positive pole is shown in Fig. 3, where t_0 is the time when the capacitor begins to discharge after the fault occurrence, and t_1 is the start time of the fault current limiting stage.

As shown in Fig. 3, the fault currents of protection installations b and a for the positive pole will have the "zero passing" characteristic for the T₁ fault area. Similarly, for the negative line fault, the fault currents of protection installations b' and a' also have the "zero passing" characteristic.

Another example is a PTP fault that occurs on T_2 . Figure 4 shows the directions of fault current flow as measured at positive pole protection installations *b* and *a*. It can be seen from Fig. 4 that for the T_2 fault area, the fault currents of protection installations *b* and *a* for the positive line will not have the "zero passing" characteristic. Similarly, for the negative line fault, the fault





Fig. 4 Faults occur on T₂



Fig. 5 Faults occur on T₃

Table 1 Fault current characteristics

Fault area/ Fault type	"zero passing" characteristic at positive pole(<i>b/a</i>)	"zero passing" characteristic at negativ pole (<i>b/a</i>)		
T ₁ /PTP	Y/Y	Y/Y		
T ₁ /PTG	Y/Y	-		
T ₂ /PTP	N/N	N/N		
T ₂ /PTG	N/N	-		
T₃/PTP	N/Y	N/Y		
T ₃ /PTG	N/Y	-		

currents of protection installations b' and a' also don't have the "zero passing" characteristic.

The PTP fault that occurs on T_3 is taken as another example to further elaborate the fault discrimination process. The directions of fault current flow measured at protection installations *b* and *a* of the positive pole are given in Fig. 5.

It can be seen from Fig. 5 that for the T_3 fault area, one fault current of protection installations *b* and *a* for the positive line satisfies the "zero passing" characteristic, whereas the other does not. The fault currents of protection installations *b*' and *a*' for the negative line fault also have the same characteristic.

2.2 The protection scheme for the fault isolation

2.2.1 Trigger criterion

The trigger criteria can be expressed as:

$$\frac{1}{m}\sum_{k=1}^{m}\left|I(k)\right| > I_{\text{set}} \, or \frac{1}{m}\sum_{k=1}^{m}\left|U(k)\right| < U_{\text{set}} \tag{3}$$

where |I(k)| and |U(k)| are the respective DC current and DC voltage amplitudes measured at protection installation *b*, *a*, *b*, *a*, and *m* = 3 are the data sampling points.

The trigger time should be earlier than the start time of the fault current limiting strategy to distinguish a fault in the stage of capacitor discharge. Moreover, the bipolar coupling effect should also be considered. Therefore, the setting I_{set} is set to 1.1 times the rated value and the setting U_{set} is set to 0.9 times the rated value.

2.2.2 Fault isolation criterion

The polarities of fault current flow measured at protection installations b and a are shown in Table 1, where "Y" indicates 'yes' and "N" indicates 'no'.

It can be seen from Table 1 that the "zero passing" characteristic of the T_1 area fault will be reflected at protection installations *b* and *a*, whereas the "zero passing" characteristic for the T_2 area fault will not exist at protection installations *b* and *a*. One of the protection installations *b* and *a* shows the "zero passing" characteristic for the T_3 area fault.

To fully consider the delay effect for the MMC control cycle [4], the duration of capacitor discharge [4], the rapidity requirements of fault identification for flexible DC transmission lines [3, 4], and sufficient margin, the identification time of the protection method is finally determined to be 3 ms. Its data window length covers the capacitor discharge duration, which meets the requirements of zero-passing discrimination of the protection method at the capacitor discharge stage.

The converter then transits from the capacitor discharge to the fault current limiting stage. Currently, the LCC side sets the trigger angle above 120° by forced phase shifting to achieve fault current limiting, while the MMC side realizes fault current limiting by setting the current reference value to 0 [4]. The above process is to extinguish the arc at the fault branch and eliminate the temporary fault.

When the fault occurs on T_3 , it is determined to be permanent, and the converter should be permanently blocked. Meanwhile, HSS isolates the fault [5]. When the fault occurs on T_1 or T_2 , it is required to identify the fault properties further. In the case of a temporary fault, the fault will be cleared when the fault current is limited to 0, while in the case of a permanent fault, the converter needs to be blocked. Therefore, it is necessary to distinguish the permanent faults in T_1 and T_2 for adaptive reclosing.

3 Fault identification scheme for adaptive reclosing

A fault identification scheme for adaptive reclosing based on an active injection strategy is introduced. The injection strategy is triggered by a fixed time delay (i.e., a generally fixed time delay of 150 ms is introduced [14]) after the fault current is limited to 0 for the fault isolation. After identifying the fault area (T_1 or T_2), MMC2 switches from the fault current limiting strategy to the active injection signal strategy.



Fig. 6 Permanent grounding fault equivalent circuit



Fig. 7 Equivalent permanent circuit with RL model

A grounding fault in the T_1 area is taken as an example, and the equivalent circuit diagram is shown in Fig. 6. U_b and I_b are the injection voltage and current flowing through the protection installation *b*, respectively. U_x and I_x are the voltage and current of the fault branch (f_1), respectively. I_g is the current flowing into the fault branch, R_g denotes the fault impedance of the fault branch, and I_c is the current flowing from the fault branch to the remote end.

3.1 The limitation of the RL model

3.1.1 Permanent fault

The equivalent permanent circuit diagram with the RL model in Fig. 6 is further represented in Fig. 7, where R_x and L_x are the equivalent resistance and inductance on the right side of the fault branch. *R* and *L* are the equivalent resistance and inductance on the left side of the fault branch, respectively.

Since the fault current is limited to 0 by the fault current limiting strategy at the remote end, the current I_c at the fault branch downstream can be approximately expressed as 0. Thus, the voltage and current calculated from the terminal b of the protection installation to the fault branch can be expressed as:

$$U_b = R_x I_b + j\omega L_x I_b + R_g I_b = x[R_l I_b + j\omega L_l I_b] + R_g I_b$$
(4)

where R_l and L_l are the resistance and inductance per unit length of the line, respectively.

The solution process for the permanent fault is given as:

$$x = \frac{\operatorname{Im}(U_b I_b^*)}{\operatorname{Im}\left\{I_b^* \left(R_l I_b + j\omega L_l I_b\right)\right\}}$$
(5)



Fig. 8 Equivalent temporary circuit with RL model



Fig. 9 Equivalent permanent circuit with distributed parameters

where Im represents the imaginary part of the complex number, and I_{h} is the conjugate of I_{h} .

The fault distance x is obtained by solving (5), and I_b in (4) can be further expressed as:

$$|I_b| = \left| \frac{U_b}{R_x + j\omega L_x + R_g} \right| > 0 \tag{6}$$

3.1.2 Temporary fault

The equivalent temporary circuit diagram with the RL model in Fig. 7 is further represented in Fig. 8, where R_w and L_w are the equivalent resistance and inductance of the whole length of the line, respectively.

Since the current I_c at the fault branch downstream can be approximately expressed as 0, the current from terminal b to terminal c can be expressed as:

$$I_b = I_c \approx 0 \tag{7}$$

Therefore, Eq. (5) can be used to determine the fault distance in the case of a permanent fault, and the amplitude of I_b is greater than 0. In the case of a temporary fault, the amplitude of I_b is equal to 0. In conclusion, the permanent fault can be identified according to the amplitude of I_{b} , and the fault distance can also be calculated.

3.1.3 Limitations

As the RL model does not consider the influence of line distribution parameters, the fault distance calculated by (4) will have large errors when the line is long. In addition, the effect of capacitive current should be considered. When a permanent fault occurs, a capacitive current occurs owing to the capacitive branch in the line after the fault branch, resulting in errors in (6). Thus, the capacitor branch makes I_b not equal to 0 in the case of a temporary fault, and (7) no longer holds.

Thus, the performance of the RL model is affected by distributed parameter effect and capacitive current. These factors will greatly impact permanent fault identification and location. In conclusion, the effect of distributed parameters and capacitive current should be considered.

3.2 The proposed method

3.2.1 Permanent fault

The proposed method fully considers the influence of the distributed parameter model and the fault branch downstream capacitive current. The equivalent circuit of where *l* denotes the whole line length.

Combining (8)-(10), the fault circuit equation when there is a permanent fault can be further represented as:

$$U_{x} - R_{g}(I_{x} - \frac{U_{x}j\omega C_{l}(l-x)}{j\omega C_{l}(l-x)[R_{l}(l-x) + j\omega L_{l}(l-x)] + 1}) = 0$$
(11)

Since (11) contains two unknowns (R_g and x), the equations of the real part and imaginary part can be listed as:

$$\begin{cases} real \left\{ U_x - R_g (I_x - \frac{U_x j \omega C_l (l-x)}{j \omega C_l (l-x) [R_l (l-x) + j \omega L_l (l-x)] + 1}) = 0 \right\} \\ imag \left\{ U_x - R_g (I_x - \frac{U_x j \omega C_l (l-x)}{j \omega C_l (l-x) [R_l (l-x) + j \omega L_l (l-x)] + 1}) = 0 \right\} \end{cases}$$
(12)

the proposed method is shown in Fig. 9, where C_l is the capacitance per unit length of the line, U_y is the voltage of the capacitor branch, and *C* is the equivalent capacitance on the left side of the fault branch.

Since the distributed parameter model takes into account the transmission line's distribution characteristics as well as the influence of distributed capacitance, the

The iterative algorithm solves the real and imaginary parts of (12) and can be finished by setting R_g and x to 0.

In the case of a metallic grounding fault, the iterative solution of (12) may have errors, requiring optimization of the initial value of $R_{\rm g}$. Therefore, Eq. (12) can be further expressed as:

$$\begin{cases} real \left\{ U_x - R_g + 0.001(I_x - \frac{U_x j \omega C_l(l-x)}{j \omega C_l(l-x) + j \omega L_l(l-x)] + 1}) = 0 \right\} \\ imag \left\{ U_x - R_g + 0.001(I_x - \frac{U_x j \omega C_l(l-x)}{j \omega C_l(l-x) + j \omega L_l(l-x)] + 1}) = 0 \right\} \end{cases}$$
(13)

voltage and current calculated from the protection installation's terminal *b* to the fault branch can be expressed as:

$$\begin{cases} U_x = U_b \cosh(\gamma x) - I_b Z_c \sinh(\gamma x) \\ I_x = I_b \cosh(\gamma x) - \frac{U_b}{Z_c} \sinh(\gamma x) \end{cases}$$
(8)

Combined with the fault circuit downstream of the fault branch, U_x and I_x can be further expressed as:

$$\begin{cases} U_x = I_g R_g \\ I_x = I_g + I_c \end{cases}$$
(9)

Since the remote system's fault current is limited to 0, it can be equivalent to an open circuit. Therefore, the fault circuit downstream of the fault branch can be expressed as:

$$\begin{cases}
I_c = \frac{U_x - U_y}{R + j\omega L} = U_y j\omega C \\
R = R_l (l - x) \\
L = L_l (l - x) \\
C = C_l (l - x)
\end{cases}$$
(10)

Given that the value of a metallic grounding fault impedance in practical projects is small but not equal to 0 under normal circumstances, optimizing the R_g value in (13) is appropriate.

3.2.2 Temporary fault

Since the fault branch does not exist, the complete voltage and current distribution exist along the line, indicating that voltage and current continuity remains after a temporary ground fault. The voltage and current of the whole line meet the distribution law along the line under the temporary fault. Therefore, the downstream branch after x_n is equivalent to the distributed parameter circuit, shown in Fig. 10, where x_n (n = 1,2,3...k) refers to the distribution points along the line corresponding to the unit length of the line.

$$\begin{array}{c} \underbrace{\begin{array}{c} \int I_{xl}U_{xk}RL & I_{xn}U_{xn} \\ X_{k} & X_{k} & X_{n} \\ I_{c} \downarrow \downarrow C & C_{l} \downarrow \downarrow I_{c_{1}} \\ C_{l} \downarrow \downarrow L_{c} & C_{l} \downarrow \downarrow C_{l} \\ \end{array}}_{a} \underbrace{\begin{array}{c} \int I_{c} \downarrow I_{c_{1}} \\ I_{c} \downarrow \downarrow L_{c} \\ b \end{array}}_{b}$$

Fig. 10 Equivalent temporary circuit with distributed parameters



Fig. 11 Equivalent temporary circuit with distributed parameters (n = k)

The corresponding voltage U_{xn} and current I_{xn} at x_n can be expressed as:

$$U_{xn} = U_b \cosh(\gamma x_n) - I_b Z_c \sinh(\gamma x_n)$$

$$I_{xn} = I_b \cosh(\gamma x_n) - \frac{U_b}{Z_c} \sinh(\gamma x_n)$$
(14)

From Fig. 10, it can be seen that the following relationships are met between I_{xn} , I_{c1} , and I_c :

$$\begin{cases} I_{xn} = I_{c1} + I_c \\ I_{c1} = U_{xn} j \omega C_l \end{cases}$$
(15)

where I_{c1} represents the current flowing into x_n .

Considering that the remote system can be equivalent to an open circuit because of its fault current being limited to 0, the fault circuit downstream of the fault branch can be expressed as:

$$\begin{cases} I_c = \frac{U_{xk} - U_{xn}}{R + j\omega L} = U_{xk}j\omega C\\ C = C_l(l - x_n)\\ R = R_l(l - x_n)\\ L = L_l(l - x_n) \end{cases}$$
(16)

From (14)-(16), the fault circuit equation when there is a temporary fault can be further expressed as:

Compared with a permanent fault at the DC line of the remote end, Eq. (11) can be further expressed as:

$$I_{xk} = \frac{U_{xk}}{R_g} \tag{19}$$

By comparing (18) and (19), it is evident that the equivalent circuit shows capacitive characteristics during a temporary fault and resistive characteristics during a permanent fault.

When using (12) to determine the fault distance in the case of a permanent fault, Eq. (19) can be further expressed as:

$$\begin{cases} real \{ U_x - R_g I_x = 0 \} \\ imag \{ U_x - R_g I_x = 0 \} \end{cases}$$
(20)

However, when (12) is used to determine the fault distance, Eq. (18) can be further expressed as:

$$\left\{\begin{array}{l} \operatorname{real}\left\{U_{x}-R'_{g}I_{x}=0\right\}\\\operatorname{imag}\left\{U_{x}-R'_{g}I_{x}=0\right\}\end{array}\Rightarrow\begin{cases}\operatorname{real}\left\{U_{x}-(-j/\omega C_{l})I_{x}=0\right\}\\\operatorname{imag}\left\{U_{x}-(-j/\omega C_{l})I_{x}=0\right\}\end{aligned}$$
(21)

where $R'_{\sigma} = -j/\omega C_l$ is the equivalent fault impedance.

Therefore, the polarity of fault calculation distance in the case of a permanent fault is opposite to that when the fault is temporary. As a result, in the case of a temporary fault, Eq. (13) indicates negative polarity when used to determine the fault distance.

$$U_{xn} - \frac{1}{j\omega C_l} (I_{xn} - \frac{U_{xn}j\omega C_l(l-x_n)}{j\omega C_l(l-x_n)[R_l(l-x_n) + j\omega L_l(l-x_n)] + 1}) = 0$$
(17)

It is evident that the fault circuit shows resistance characteristics under permanent fault and capacitance characteristics under temporary fault by comparing (17) and (11). Therefore, the polarity of fault calculation distance when there is a permanent fault is opposite to that when it is temporary. The polarity characteristics for fault distance are further explained below.

To simplify the analysis, the x_k point is selected (n=k), and the equivalent circuit diagram is shown in Fig. 11.

As can be seen from Fig. 11, when x_k is selected (n = k), Eq. (17) can be further expressed as:

$$I_{xk} = U_{xk} j \omega C_l \tag{18}$$

3.3 Active injection signal strategy 3.3.1 *Generation of signal*

After a fixed delay, MMC2 injects a specific frequency signal to the line by setting a specific frequency reference value to U_{dcset} . The process is shown in Fig. 12.

As illustrated in Fig. 12, U_{dcref} and U_{dcset} are the respective references and set values of the DC side voltage, while V_{refpm} and V_{refnm} are the voltage reference



Fig. 12 Injection signal process

values of the upper and lower bridge arms, respectively. N_p and N_n are the sub-modules in the upper and lower bridge arms, respectively. NLM denotes nearest level modulation, u_m represents the equivalent value of the differential-mode voltage, and $U_{\rm cn}$ represents the sub-module capacitance voltage.

From Fig. 12, by setting U_{dcset} , the control of the submodules can be realized to inject the signal. The reference value of U_{dcset} is shown as:

$$U_{\rm dcset} = 0.1 U_{\rm dcn} \sin \left[\omega (t - t_1) \right] t_1 \le t \le t_2$$
(22)

where t_1 is the beginning time in the case of signal injection, and t_2 is the finishing time. U_{dcn} represents the rated value of the DC voltage.

3.3.2 Amplitude of injection signal

The injection signal amplitude should be large enough to be identifiable to increase the proposed method's performance. The amplitude of the injection signal should consider the measurement unit, the influence of the injection signal on the injection equipment, and the amplitude output capabilities of the converter. The details are:

- (a) The influence of the measurement unit. In general, the lower limit of the electronic current and voltage transformer is larger than 0.05 p.u. [21]. This is required to guarantee that the amplitude of the injection signal is larger than the lower limit range of the measurement for the injection signal.
- (b) The influence of the injection signal on the injection equipment. It is necessary to avoid the capacitor voltage exceeding the voltage borne by the IGBT reverse parallel diode in the case of signal injection, shown as:

$$U_{c_{rms}} \leq U_{VT_{rms}}, U_{c_{peak}} \leq U_{VT_{peak}}$$
$$U_{c_{rms}} = \sqrt{(U_c)^2 + \sum_{h=1}^{\infty} (U_c^h)^2/2}$$
$$U_{c_{peak}} = U_c + \max |\Delta U_c|$$
(23)

where subscripts "c" and "VT" refer to a sub-module capacitor and IGBT reverse parallel diode, respectively. The subscripts "rms" and "peak" represent the effective and peak values, respectively. The superscript "*h*" represents the harmonic frequency, and U_c represents the DC value of the capacitor voltage of the sub-module. ΔU_c indicates the fluctuation of the capacitor voltage of the sub-module compared with the rated value.

In the process of injecting the signal, the amplitude of the injection signal is small, and the influence on the fluctuation of capacitor voltage is limited. The capacitor voltage fluctuation rate can be expressed as:

$$\varepsilon = \frac{\max |\Delta U_{\rm c}|}{U_{\rm c}} \tag{24}$$

Considering the cost of capacitors and power devices [22], the reasonable value range is about 0.1 to 0.15 p.u. The converter usually adopts the sub-module voltage balancing control strategy, and the capacitor voltage fluctuation component of its sub-module is much less than 0.15 p.u. It is within the rated range of the sub-module.

(iii) The amplitude output capability of the converter. It is essential to assess the capacitor voltage output capabilities of the sub-module owing to the signal injection operation. According to the DC voltage operating range of the hybrid MMC [4], the voltage output range of the signal output by the converter meets the following requirements:

$$M_{\rm ac} - \frac{2N_f}{N} \le U_{\rm dcref} \le \frac{2N_f}{N} - M_{\rm ac}$$
(25)

where $M_{\rm ac}$ is AC voltage modulation, N is the total number of converter modules, and $N_{\rm f}$ is the number of full bridge sub-modules.

When the number of full bridge sub-modules accounts for half of the total sub-modules, the voltage signal output range by the port converter is ± 0.1 p.u. Therefore, it should be ensured that the amplitude of the voltage output by the converter should not exceed 0.1 p.u.

In conclusion, it is recommended that the amplitude of the injection signal should not exceed 0.1 p.u.

3.3.3 Frequency of injection signal

- (a) The frequency should be lower than the data sampling rate and the control frequency of the converter sub-module [24].
- (b) The influence of frequency output capacity of the converter. The tracking process error of the converter control influence on the injection signal needs to be considered. The change process of the converter control effect on the injection signal meets the following requirements:

$$\frac{\mathrm{d}U_{\mathrm{dcref}}}{\mathrm{d}t} \le \frac{u_{\mathrm{c}}}{T_{\mathrm{c}}} \tag{26}$$



Fig. 13 Transmission coefficient of line

where $T_{\rm c}$ is the control cycle of MMC.

Taking the AC injection signal as an example, its form can be expressed as:

$$U_{\rm dcref} = A \sin 2\pi f_{\rm s} t \tag{27}$$

where f_s and A are the frequency and amplitude of the given reference value, respectively.

A control cycle when the given reference value waveform changes fastest (steepest) changes a level to ensure the waveform quality of the injection signal. At this time, the frequency of the injection signal is:

$$f_{\rm s} \le \frac{1}{2\pi ANT_{\rm c}} = f_{\rm min} \tag{28}$$

It can be seen from (28) that it is required to guarantee that the injection signal should be less than f_{\min} to make the output injection signal reflect the given reference value.

(iii) It is necessary to consider the attenuation factor of the injection signal in the transmission process. The transmission coefficient of the line can be expressed as:

$$A_L(j\omega) = \exp[-\gamma(j\omega)l]$$
⁽²⁹⁾

The relationship between transmission coefficient amplitude, line length, and frequency is shown in Fig. 13.

From Fig. 13, it can be seen that the frequency should not exceed 50 Hz (i.e., in the case of a 500 km length line, the amplitude attenuation exceeds 0.1 p.u).

In conclusion, it is recommended that the frequency of the injection signal can be set to 50 Hz.

3.3.4 Length of the injection signal

(a) From the Fourier algorithm, the length of the injection signal should be greater than the data window length of 50 Hz. (b) The injection signal should be assured to have a certain duration and be longer than the open-loop control regulation period to mitigate the effect of the system's open-loop control regulation process. The corresponding open-loop control adjustment time generally can be expressed as [23]:

$$T_{\rm d} \approx \left(1 + \frac{1}{\omega^2}\right) \frac{8\omega^2 L_{\rm arm}^2 C_{\rm arm}}{NR_{\rm arm}}$$
 (30)

where ω is the frequency of the injection signal, and $C_{\rm arm}$ denotes the capacitance of the bridge arm.

Therefore, the length of the injection signal should be greater than the corresponding length of $T_{\rm d}$.

(iii) Considering that the frequency of the injection signal is 50 Hz, the signal length should be at least an integral multiple of the frequency of the injection signal. A corresponding margin range should be reserved to identify the permanent fault and location reliably. The length of the injection signal is selected as twice the data length of 50 Hz.

Finally, combined with the above analysis, the length is suggested to be 40 ms.

4 The process of the proposed scheme

For the fault identification scheme, the implementation steps are as follows.

1. The fault isolation scheme uses the currents at the protection installations *b* and *a* at the capacitor discharge stage to realize fault discrimination by the "zero passing". The details are described below.

The currents at the protection installations b and a will have the "zero passing" characteristic under the T₁ area fault scenarios. In contrast, the currents at the protection installations b and a will not have the "zero passing" characteristic under the T₂ area fault scenarios. In the case of T₃ area faults, the current at one of protection installations b and a has the "zero passing" characteristic.

When the fault occurs on T_3 , it is determined to be permanent, the DC system blocks the converter, and HSS isolates the fault. When the fault occurs on T_1 or T_2 , it is required to identify the fault properties further. Therefore, it is necessary to distinguish the permanent faults in T_1 and T_2 for adaptive reclosing.

2. After a 150 ms fixed time delay, the characteristic signal is injected into the line by MMC2. The fault circuit is equivalent to the distributed parameter model, and the fault distance is solved by (13). U_x and I_x



Fig. 14 The calculation process of TRR

denote the electrical quantity of positive or negative pole, which need to be decoupled in (8) as:

$$U_{x(0,1)} = U_{b(0,1)} \cosh(\gamma_{(0,1)} x) - I_{b(0,1)} Z_c \sinh(\gamma_{(0,1)} x)$$

$$I_{x(0,1)} = I_{b(0,1)} \cosh(\gamma_{(0,1)} x) - \frac{U_{b(0,1)}}{Z_c} \sinh(\gamma_{(0,1)} x)$$

(31)

where the subscripts "1" and "0" denote 1 mode and 0 mode, respectively.

 U_x and I_x can be further expressed as:

$$\begin{bmatrix} U_{xp} \\ U_{xn} \end{bmatrix} = \frac{\sqrt{2}}{2} \begin{bmatrix} 11 \\ 1-1 \end{bmatrix} \begin{bmatrix} U_{x1} \\ U_{x0} \end{bmatrix}$$
(32)

$$\begin{bmatrix} I_{xp} \\ I_{xn} \end{bmatrix} = \frac{\sqrt{2}}{2} \begin{bmatrix} 11 \\ 1-1 \end{bmatrix} \begin{bmatrix} I_{x1} \\ I_{x0} \end{bmatrix}$$
(33)

where the subscripts "p" and "n" denote the positive pole and negative pole, respectively.

The Trust Region Reflection (TRR) algorithm is widely used to solve nonlinear equations because it does not depend on the influence of initial value [26]. The calculation process of the TRR algorithm is shown in Fig. 14.

The TRR algorithm is used to solve (13) to get the fault distance. The initial values of $[x, R_g]$ can be set to [0, 0]. When the fault distance exceeds 0, it is identified as a permanent fault, and the fault distance is the fault location. When the fault distance is less than 0, it



Fig. 15 Fault identification scheme flow chart

is judged as a temporary fault. The process of permanent fault identification is as follows:

Permanent fault:
$$x > 0$$

Temporary fault: $x < 0$ (34)

According to (34), the proposed method does not need to set the setting values through simulation and ensures the reliability and sensitivity of fault identification in principle.

Given the fault impedance in the case of non-pure resistive characteristics (i.e., the resistance-inductance characteristic [27] or time-varying resistance characteristic [29]), the fault location accuracy may be





Table 2 Parameters of the hybrid multi-terminal HVDC system

Parameter	Value
MMC rating capacity	400 MVA
LCC rating capacity	800 MVA
Rated voltage of the DC side	400 kV
Smoothing Reactor (LCC)	300 mH
Smoothing Reactor (MMC)	100 mH
AC system voltage (LCC)	230 kV
Transformation ratio (LCC)	525/210 kV
AC voltage (MMC)	353 kV
Transformation ratio (MMC)	230/260 kV
Short-circuit impedance	18%
N _{HB} /N _{FB}	100/100
Inductance of arm	40 mH
Capacitance of arm	25 mF
DC line length	500 km
Sampling frequency	10 kHz
Time of the failure	1 s

affected by the non-pure resistance part. However, fault impedance generally presents resistive characteristics [28]. Therefore, the fault impedances in permanent and temporary faults have resistive and capacitive characteristics, respectively, as shown in (17) and (11). The fault location results still have polarity differences, and the fault properties can still be identified theoretically. When the permanent fault is identified, HSS isolates the fault line. When it is judged as a temporary fault, the system restarts.



Fig. 17 f_{1-30} (Permanent fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 18 *f*₁₋₃₀ (Temporary fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 19 f_{1-250} (Permanent fault). **a** Zero passing characteristics. **b** DC voltage







Fig. 21 f_{1-500} (Permanent fault). a Zero passing characteristics. b DC voltage

To sum up, the fault identification scheme flow chart is illustrated in Fig. 15. As seen, the signal can be injected several times to improve the reliability of permanent fault identification. The number of injections is set at 2 in this paper.



Fig. 22 *f*₁₋₅₀₀ (Temporary fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 23 f_{2-30} (Permanent fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 24 *f*₂₋₃₀ (Temporary fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 25 f_{2-250} (Permanent fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 26 *f*₂₋₂₅₀ (Temporary fault). **a** Zero passing characteristics. **b** DC voltage

5 Simulation

A bipolar hybrid multi-terminal HVDC system model is developed, as illustrated in Fig. 16a, and the system parameters are shown in Table 2. The frequency-dependent line model is shown in Fig. 16b. The fault occurs at 1 s, and the temporary fault duration is 0.01 s.



Fig. 27 f₂₋₅₀₀ (Permanent fault). a Zero passing characteristics. b DC voltage



Fig. 28 f_{2-500} (Temporary fault). **a** Zero passing characteristics. **b** DC voltage



Fig. 29 f_3 (Permanent fault). **a** Zero passing characteristics. **b** DC voltage

5.1 Performance of fault identification scheme

The pole-to-pole (PTP) fault is the most serious type of DC line fault, so the simulation example takes the PTP fault to test the proposed fault identification scheme. The fault locations are T₁, T₂, and T₃, respectively. The fault locations of T₁ are 30 km, 250 km, and 500 km away from the terminal b end (f_{1-30} , f_{1-250} , f_{1-500}), whereas the fault locations of the T₂ area are 30 km, 250 km, and 500 km away from terminal a, (f_2 - $_{30}$, f_{2-250} , f_{2-500}). The fault properties are temporary and permanent faults. The "zero passing" characteristic of positive pole currents at terminals b and a, and the measurement results of the voltage of terminal b corresponding to the positive pole are shown in Figs. 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28 and 29. The simulation results of the proposed scheme are summarized in Table 3.

It can be seen from Table 3 that the "zero passing" characteristics can be used to detect the fault area and realize fault isolation rapidly. The proposed fault identification scheme can calculate the accurate fault distance and identify the fault properties.

Fault area/properties (P or T)	Zero passing characteristics (<i>b/a</i>)	Fault isolation results	Fault distance (km)	Permanent fault?	
f ₁₋₃₀ /P	Y/Y	T ₁	29.98	Y	
f ₁₋₃₀ /T	Y/Y	T ₁	- 959.96	Ν	
f ₁₋₂₅₀ /P	Y/Y	T ₁	248.87	Y	
f ₁₋₂₅₀ /T	Y/Y	T ₁	- 961.34	Ν	
f ₁₋₅₀₀ /P	Y/Y	T ₁	499.71	Y	
f ₁₋₅₀₀ /T	Y/Y	T ₁	- 969.98	Ν	
f ₂₋₃₀ /P	N/N	T ₂	30.00	Y	
f ₂₋₃₀ /T	N/N	T ₂	- 945.85	Ν	
f ₂₋₂₅₀ /P	N/N	T ₂	249.54	Y	
f ₂₋₂₅₀ /T	N/N	T ₂	- 967.64	Ν	
f ₂₋₅₀₀ /P	N/N	T ₂	498.66	Y	
f ₂₋₅₀₀ /T	N/N	T ₂	- 973.41	Ν	
f ₃ /P	N/Y	T ₃	-	Y	

 Table 3
 Simulation results of the proposed scheme



Fig. 50 T_{1-30} (500 12). a Zero passing characteristics. b DC voltage



Fig. 31 f_{1-470} (300 Ω). a Zero passing characteristics. b DC voltage



Fig. 32 f_{2-30} (300 Ω). a Zero passing characteristics. b DC voltage



Fig. 33 f_{2-470} (300 Ω). a Zero passing characteristics. b DC voltage

 Table 4
 Performance of anti-pure-resistive fault impedance

Fault area	Zero passing characteristics(<i>b/a</i>)	Fault isolation results	Fault distance (km)	Permanent fault?
f ₁₋₃₀	Y/Y	T ₁	30.32	Y
f ₁₋₄₇₀	Y/Y	T ₁	467.90	Y
f ₂₋₃₀	N/N	T ₂	29.75	Y
f ₂₋₄₇₀	N/N	T ₂	466.51	Y



Fig. 34 *f*₁₋₂₅₀ (Permanent fault & time-varying fault impedance). **a** Zero passing characteristics. **b** DC voltage



Fig. 35 f_{1-250} (Temporary fault & time-varying fault impedance). **a** Zero passing characteristics. **b** DC voltage

5.2 Performance of anti-fault impedance *5.2.1 Pure resistive fault impedance*

The simulation conditions of the fault identification scheme for performance verification are permanent poleto-ground (PTG) faults, and the fault impedance is 300



Fig. 36 f_{1-500} (Permanent fault & time-varying fault impedance). **a** Zero passing characteristics. **b** DC voltage



Fig. 37 *f*₁₋₅₀₀ (Temporary fault & time-varying fault impedance). **a** Zero passing characteristics. **b** DC voltage

Ω. The fault locations are f_{1-30} , f_{1-470} , f_{2-30} , and f_{2-470} . The "zero passing" characteristic of positive pole currents at terminals *b* and *a*, and the measurement results of the voltage of terminal *b* corresponding to the positive pole are shown in Figs. 30, 31, 32 and 33. The performance of anti-pure-resistive fault impedance is shown in Table 4.

It can be seen from Table 4 that the fault area can be identified at high fault impedance by using the "zero passing" characteristic, which has strong anti-fault impedance performance. The proposed fault identification scheme can effectively identify fault properties and is largely unaffected by fault impedance. Its location accuracy can be generally maintained within a 1% error range.

5.2.2 Time-varying fault impedance

The fault impedance can be affected by wind speed or direction, air humidity, working condition change and other factors, so it may have time-varying characteristics [29]. The fault area is selected as T_1 , and the fault locations are set as 250 km and 500 km away from terminal b (f_{1-250} , and f_{1-500}) to verify the performance of the proposed scheme in a time-varying fault impedance scenario. The time-varying fault impedance is set as $R_f = 180 + 60t \ \Omega$ ($t > t_{fault}$, where t_{fault} is the time corresponding to the initial instant of the fault). The "zero passing" characteristic of positive pole currents at terminals b and a, and the measurement results of the voltage of terminal b corresponding to the positive pole are shown in Figs. 34, 35, 36, 37. The performance of anti-time-varying fault impedance is shown in Table 5.

It can be seen from Table 5 that the fault area can be identified at higher fault impedance by using the "zero passing" characteristic, which has a certain anti-timevarying fault impedance performance. Although the proposed method has some location errors due to the influence of time-varying fault impedance, it can effectively distinguish the fault properties and achieve the function of adaptive reclosing.

Fault area/Fault properties(P/T)	Zero passing characteristics(<i>b</i> / <i>a</i>)	Fault isolation results	Fault distance (km)	Permanent fault?	
f ₁₋₂₅₀ (P)	Y/Y	T ₁	247.87	Y	
f ₁₋₂₅₀ (T)	Y/Y	T ₁	- 958.84	Ν	
f ₁₋₅₀₀ (P)	Y/Y	T ₁	517.68	Y	
$f_{1-500}(T)$	Y/Y	T ₁	- 1022.41	Ν	

 Table 5
 Performance of anti-time-varying fault impedance

 Table 6
 Performance of noise interference

Fault area/ properties(P/T)	Zero passing characteristics(<i>b</i> / <i>a</i>)	Fault isolation results	Fault distance (km)	Permanent fault?
f ₁₋₁₀ /P	Y/Y	T ₁	10.34	Y
f ₁₋₅₀₀ /P	Y/Y	T ₁	496.16	Y
f ₂₋₁₀ /P	N/N	T ₂	10.12	Y
f ₂₋₅₀₀ /P	N/N	T ₂	495.88	Y
<i>f</i> ₁₋₁₀ /T	Y/Y	T ₁	- 975.65	Ν
f ₁₋₅₀₀ /T	Y/Y	T ₁	- 981.21	Ν
f ₂₋₁₀ /T	N/N	T ₂	- 978.64	Ν
f ₂₋₅₀₀ /T	N/N	T ₂	- 977.13	Ν

Fault area/sampling rates	Zero passing characteristic (<i>b/a</i>)	Fault isolation results	Fault distance (km)	Permanent fault?
f ₁₋₃₀ /5 kHz	Y/Y	T ₁	- 959.82	N
f ₁₋₄₇₀ /5 kHz	Y/Y	T ₁	- 966.58	Ν
f ₁₋₃₀ /15 kHz	Y/Y	T ₁	- 964.37	Ν
f ₁₋₄₇₀ /15 kHz	Y/Y	T ₁	- 969.56	Ν
f ₁₋₃₀ /20 kHz	Y/Y	T ₁	- 967.05	Ν
f ₁₋₄₇₀ /20 kHz	Y/Y	T ₁	- 977.64	Ν

Table 7 Performance of different sampling rates

Table 8 Performance of different DC boundary strengths

Fault area/ CLR(LCC/MMC) (mH)	Zero passing characteristics(<i>b/a</i>)	Fault isolation results	Fault distance (km)	Permanent fault?
f ₁₋₃₀ /(100/10)	Y/Y	T ₁	29.46	Y
f ₁₋₃₀ /(200/50)	Y/Y	T ₁	29.65	Y
$f_{1-30}/(300/100)$	Y/Y	T ₁	29.98	Y
$f_{1-470}/(100/10)$	Y/Y	T ₁	468.65	Y
$f_{1-470}/(200/50)$	Y/Y	T ₁	468.74	Y
$f_{1-470}/(300/100)$	Y/Y	T ₁	470.41	Υ

5.3 Performance of noise interference

Temporary and permanent positive PTG faults are selected for simulation conditions. The noise intensity is 30 dB, and the fault impedance is 300 Ω . The fault locations are f_{1-10} , f_{1-500} , f_{2-10} , and f_{2-500} . The performance of noise interference is shown in Table 6.

From Table 6, it can be seen that noise interference only has a small influence on the "zero passing" characteristic. Consequently, the proposed fault identification system can effectively identify faults in the fault isolation stage. The proposed scheme accomplishes permanent fault identification by calculating the fault distance in the adaptive reclosing stage and has strong anti-interference performance.

Table 9	Performance	comparison	with protec	tion methods
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5.4 Performance of different sampling rates

Temporary PTP faults are chosen for the simulation scenario. The sampling rates are selected as 5 kHz, 15 kHz and 20 kHz, and the fault locations are set as f_{1-30} and f_{1-470} . The performance at different sampling rates is compared in Table 7.

Table 7 shows that the proposed method is largely unaffected by the sampling rate since it uses the zeropassing characteristics of the T-shaped area rather than the traveling wavefront characteristics.

5.5 Performance at different DC boundary strengths

Permanent PTP faults are selected for simulation. In combination with the selection of current-limiting reactors (CLR) values in the literature [3, 6–9], the CLR values at the LCC side are set to 100 mH, 200 mH, and 300 mH, respectively, while the CLR values at the MMC side are set to 10 mH, 50 mH, and 100 mH, respectively. The fault locations are set as f_{1-30} and f_{1-470} . The performance of different DC boundary strengths is shown in Table 8.

From Table 8, it can be seen that the proposed method is largely unaffected by different DC boundary values because it uses the zero-passing characteristics of the T-shaped area rather than the DC boundary attenuation effect characteristics.

Method	Method theory	Sampling rate required	Depend on wavefront identification?	Depend on the DC boundary?	Depend on advanced algorithms?	Data transmission delay?
[6]	Traveling wave	100 kHz	Yes	Yes	Yes	_
[7]		400 kHz	Yes	Yes	Yes	-
[8]		80 kHz	Yes	Yes	Yes	-
[3]		1 MHz	Yes	Yes	Yes	Yes
[10]		1 MHz	Yes	Yes	Yes	Yes
[11]		10 kHz	No	No	Yes	Yes
[12]		50 kHz	Yes	Yes	Yes	Yes
[9]	Fault analysis	10 kHz	No	Yes	Yes	_
Proposed method		≥5 kHz	No	No	No	No

Method	Injection equipment	System	Core theory	Sampling rates	Fault impedance	Depend on wavefront identification?	Depend on the DC boundary?
[13]	Additional device	MTDC	Traveling wave	50 kHz	10 Ω	Yes	Yes
[14]	MMC	AC system		1 MHz	100 Ω	Yes	Yes
[15]	MMC	DC system		10 kHz	300 Ω	Yes	Yes
[16]	LCC	Hybrid HVDC system		50 kHz	100 Ω	Yes	Yes
[17]	DCCB	MTDC		50 kHz	200 Ω	Yes	Yes
[18]	DCCB	MTDC		10 kHz	200 Ω	Yes	Yes
[19]	Wind power	AC system	Fault analysis	20 kHz	50 Ω	No	No
[20]	DCCB	MTDC		10 kHz	300 Ω	No	No
Proposed method	ММС	Hybrid MTDC		≥5 kHz	300 Ω	No	No

Table 10 Performances comparison with adaptive reclosing methods

5.6 Advantages of the proposed scheme

This section compares the performance of the hybrid multi-terminal HVDC transmission system protection methods [3, 6–12] and adaptive reclosing methods [13–20] with the proposed scheme, as Tables 9 and 10 compare the performance for protection and for adaptive reclosing, respectively.

As is seen, the proposed method differs from singleend traveling wave protection principles and is less affected by the influence of DC boundary and sampling rate. It uses the current zero-passing characteristics of the T-shaped region in the hybrid multi-terminal DC transmission system to identify the fault area quickly without complex mathematical calculations. The method is different from the traditional pilot principles. It takes advantage of the current zero-passing characteristics in the T-shaped area, and is less affected by the communication and calculation delays at both ends of the DC line.

Compared with the existing injection permanent fault identification methods, the proposed method has the following advantages:

- The influence of the downstream branch capacitive current of the fault branch is fully considered. Therefore, fault property identification and permanent fault location are realized by solving the fault distance under the distributed parameter model through the TRR algorithm.
- The proposed method significantly differs in fault distance between temporary and permanent faults, does not need to set the setting values via simulation, and has high sensitivity in fault discrimination. It also has the function of permanent fault location.
- Unlike traveling wave front identification methods, it is less affected by the sampling rate, fault impedance, DC boundary and other factors.

6 Conclusion

Through theoretical and simulation verification for the proposed fault identification scheme, the following conclusions can be drawn:

- In the protection stage, the "zero-passing" characteristics of the current at the local end during the capacitor discharge stage are used to quickly identify the fault area without a long communication delay and complex mathematical calculation. It can achieve fault isolation by combining the fault current limiting strategy with HSS.
- In the adaptive reclosing stage, the proposed method is realized by solving the fault distance under the distributed parameter model through the TRR algorithm. It can sensitively identify the fault properties and has the fault location function. Moreover, it does not need to set the setting values via simulation.
- The proposed fault identification scheme is suitable for long transmission lines during the whole fault process and has strong anti-fault impedance and anti-interference performance. Furthermore, it is less affected by the DC boundary and sampling rate than existing methods.

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Authors' information

Junjie Hou (1993-), born in Xinjiang, China. He received the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2022. He is currently a Assistant Professor with the School of Electrical Engineering, Xinjiang University. His research interests include transmission line fault location and protections.

Guobing Song (1972-), born in Henan, China. He received the Ph.D. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2005. He is currently a Professor with the School of Electrical Engineering, Xi'an Jiaotong University and the School of Electrical Engineering, Xinjiang University. His research interests include transmission line fault location and protections.

Yanfang Fan (1971-),born in Xinjiang, China. She received the master degree in electrical engineering from Dalian University of Technology, Dalian, China, in 2001. She is currently a Professor with the School of Electrical Engineering, Xinjiang University. Her research interests include power system relay protection technology and renewable energy grid connection technology.

Author contributions

JH, as the first author and corresponding author, contributed significantly to the research, writing, and submission of the paper. GS, as the second author, contributed significantly to analysis and supervised the research of the paper. YF as the third author, contributed significantly to make the paper more comprehensible and grammatically correct. All the authors read and approved the submitted manuscript.

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Availability of data and materials

The relevant data discussed in this paper can only be considered for sharing if a sincere request is extended to the corresponding author.

Declarations

Competing interests

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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